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MS-7695 Ver:1.0

CPU:

AMD FM1

System Chipset:

AMD - Hudson D3

On Board Chipset:

LPC Super I/O --F71889

LAN-Realtek 8111E

Azalia CODEC - Realtek ALC892

Main Memory:

DDR III * 4 (max 32G)

Expansion Slots:

PCI Express X16 Slot * 2

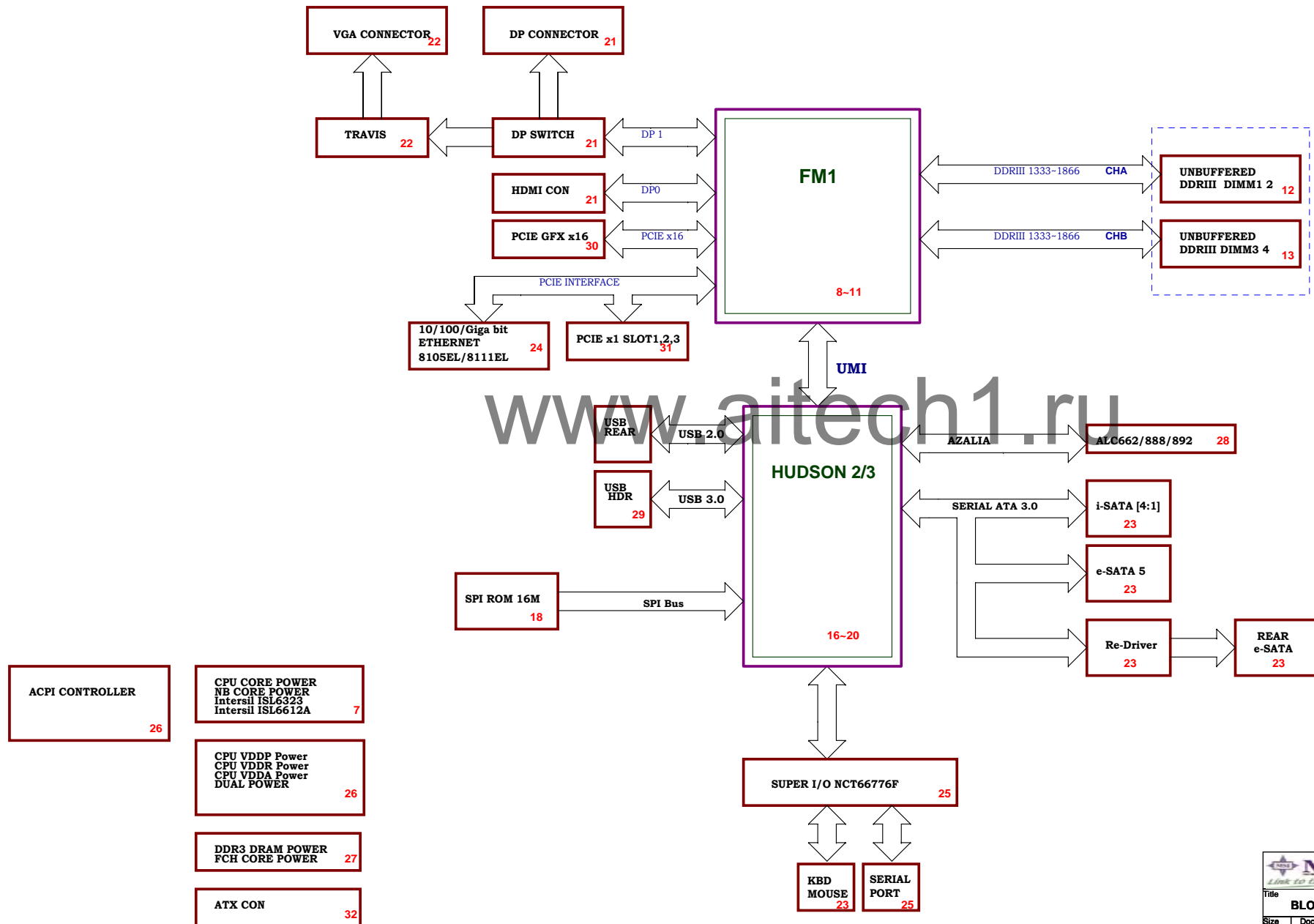
PCI Express X1 Slot * 1

PCI Slot * 1

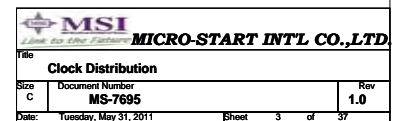
VRM

Controller - Intersil ISL6328 4+1 Phase

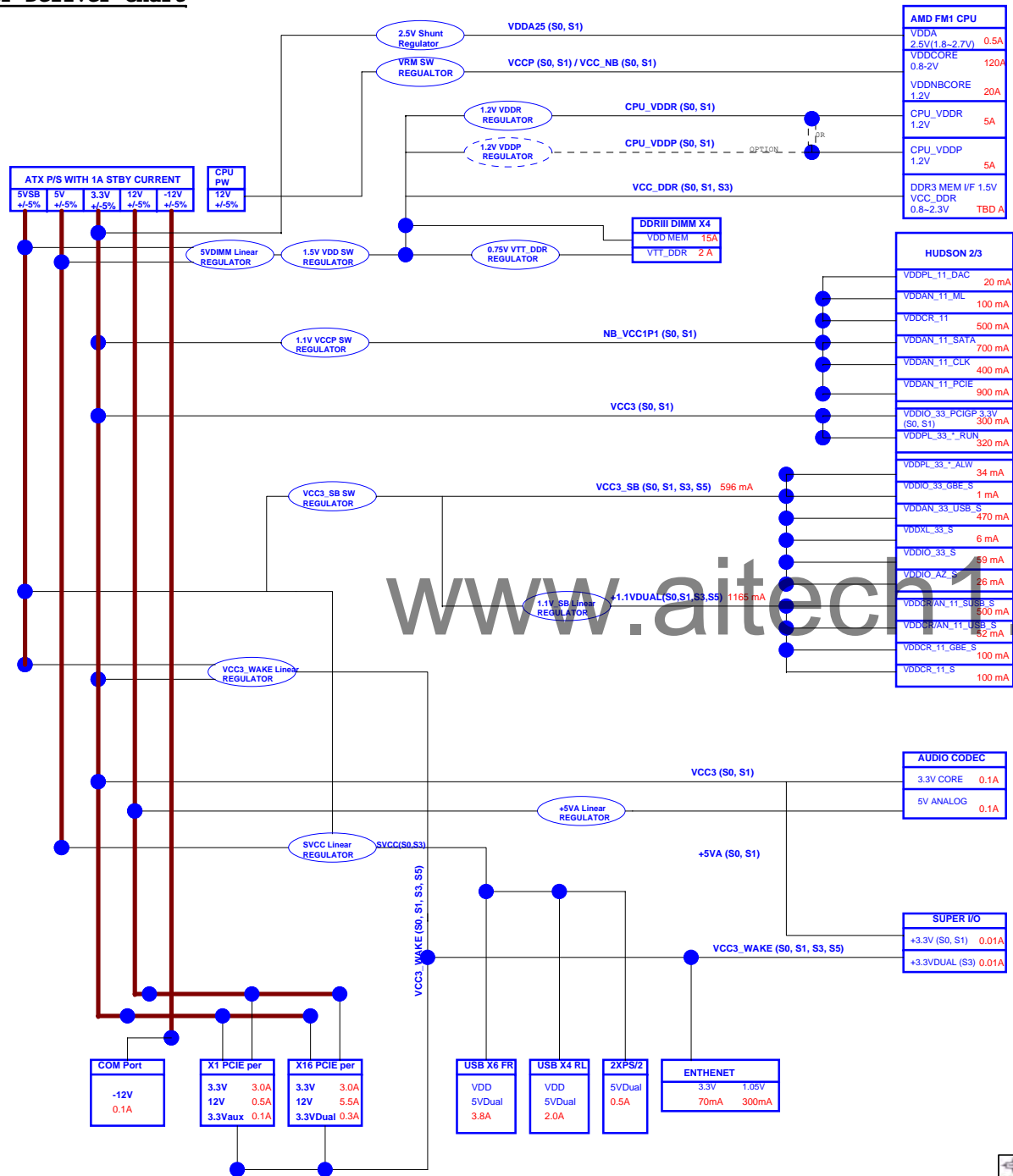
FUSION BLOCK DIAGRAM




INTERNAL CLOCK MODE

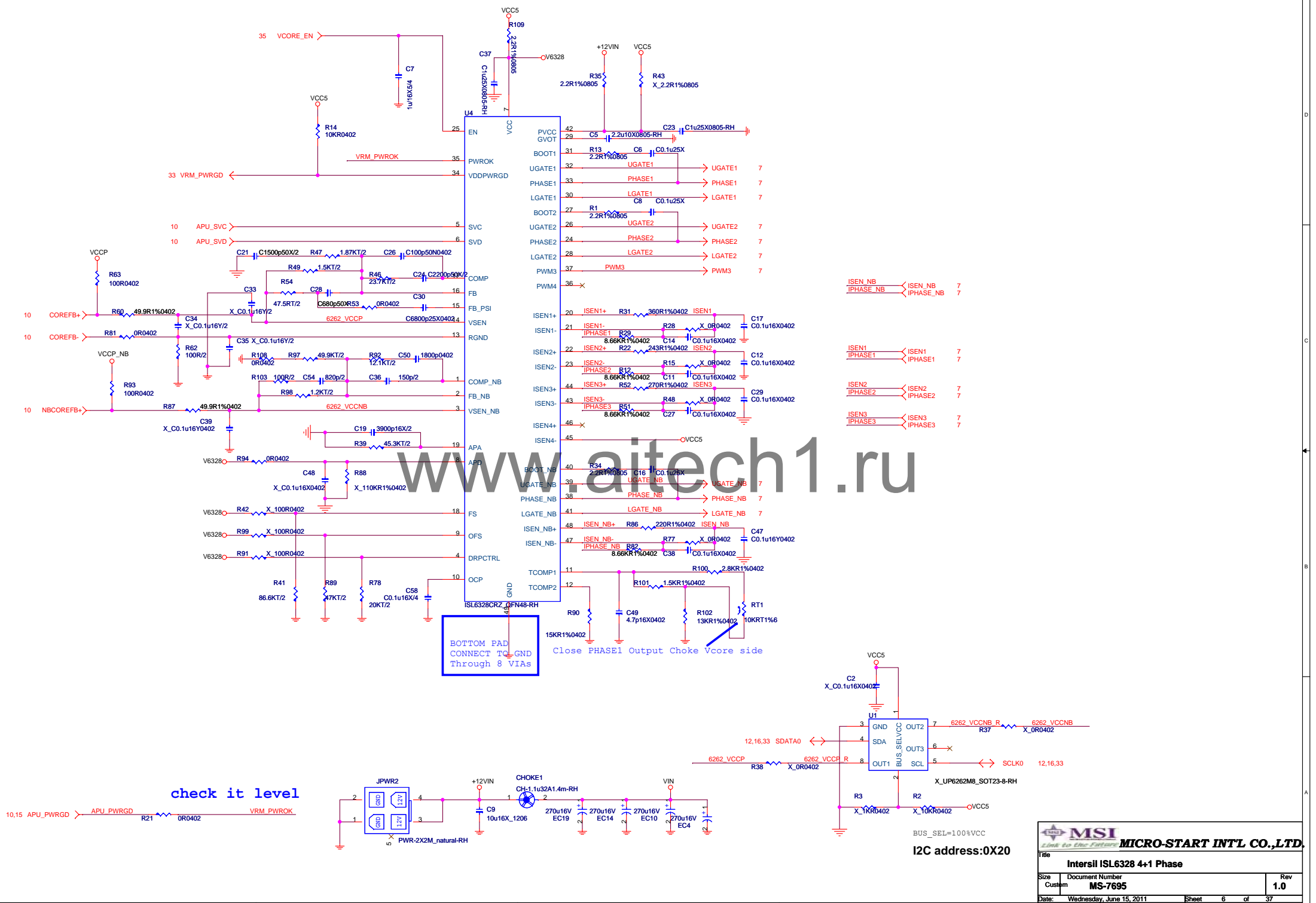


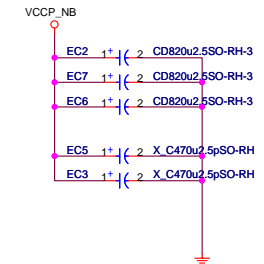
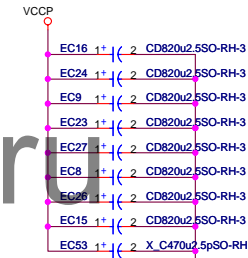
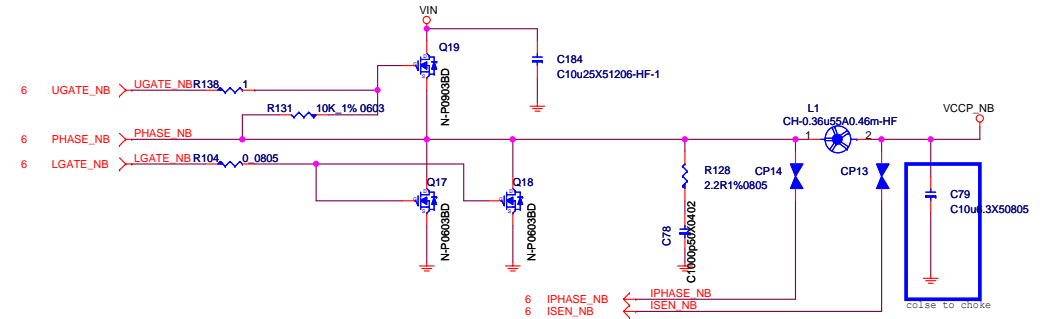
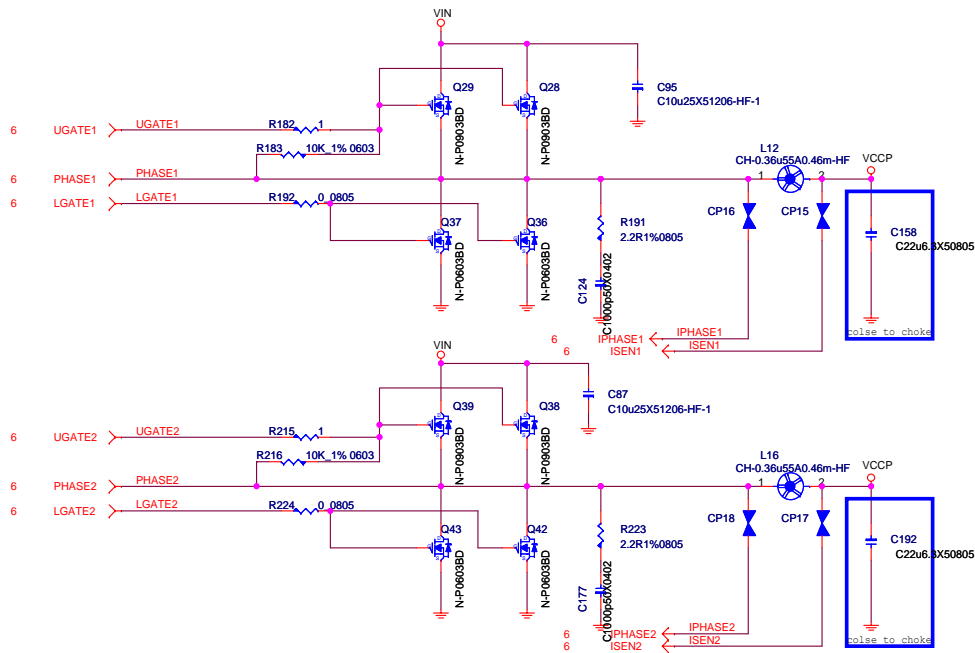
Power Deliver Chart



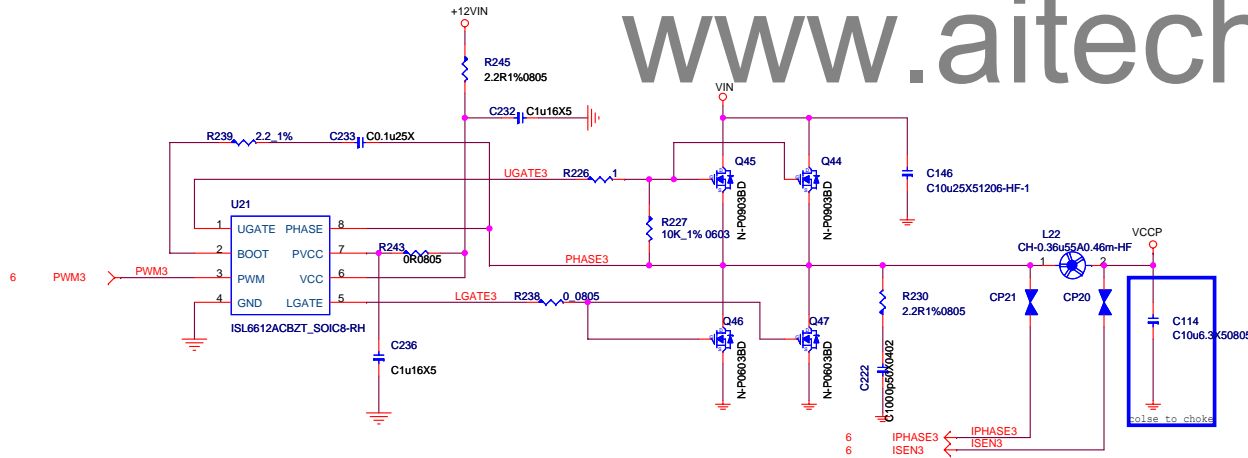
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<div><div><div><div>MSI</div><div><small>MICRO-STAR INTERNATIONAL</small></div></div><div><i>Link to the Future</i></div></div><div>MICRO-START INT'L CO.,LTD.</div></div>			
Title			
RESET MAP			
Size	Document Number		Rev
A	MS-7695		1.0
Date:	Tuesday, May 31, 2011	Sheet	5 of 37



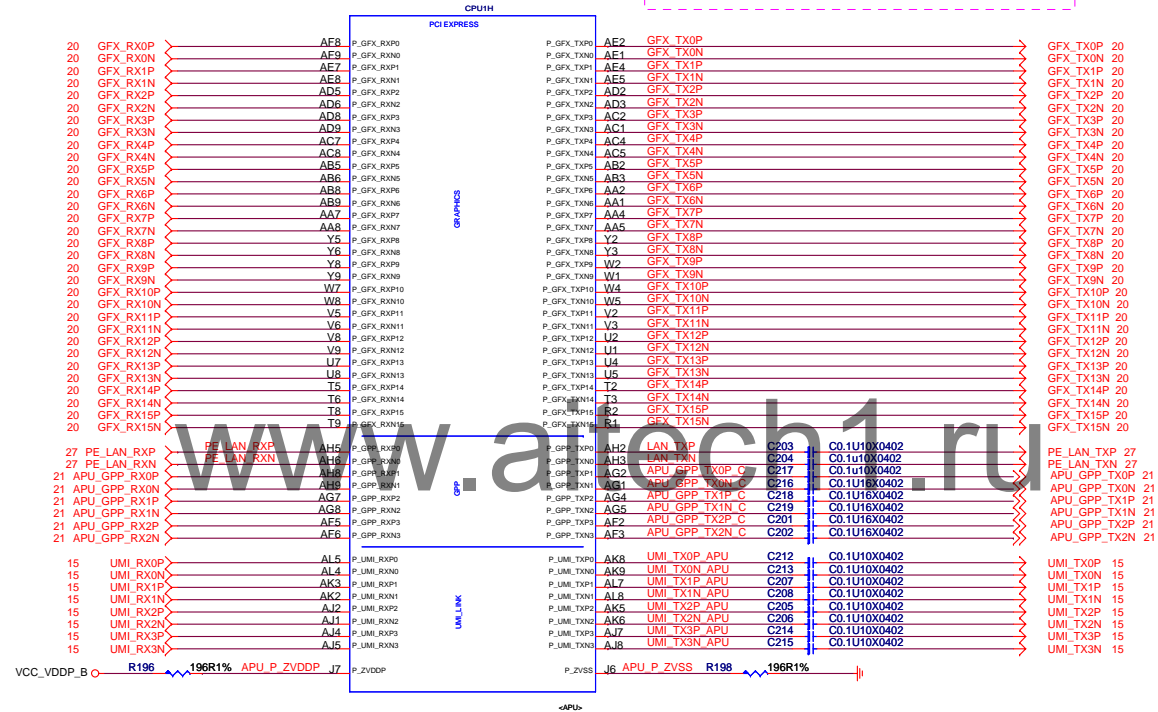


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FM1 PCIE I/F

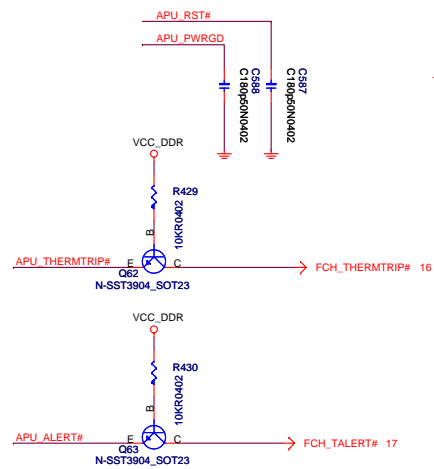
mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%



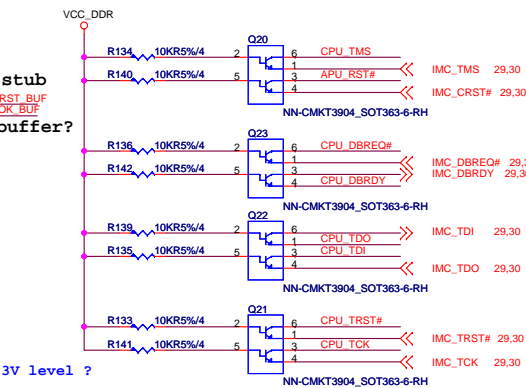
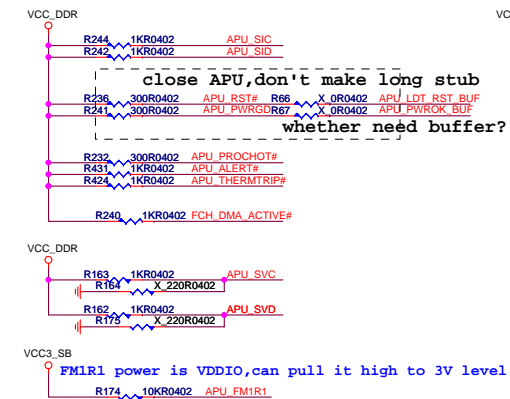
For DVI/HDMI

For VGA

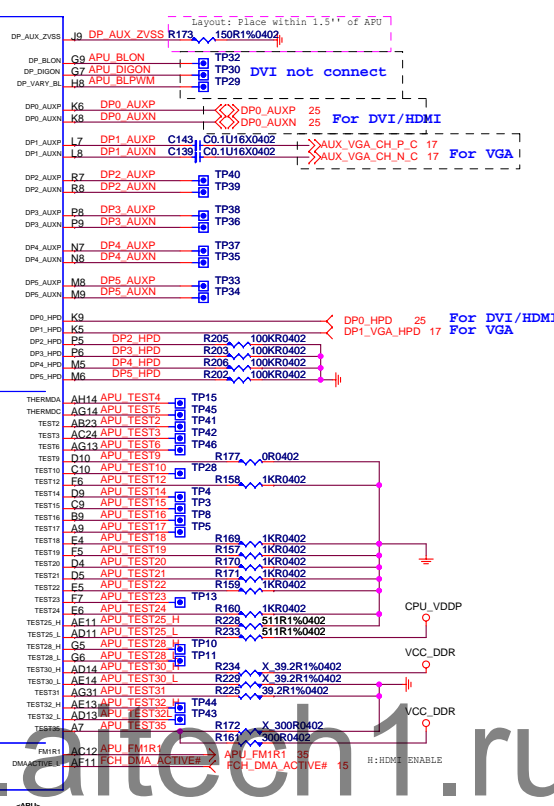
check it level to VRM PWROK



PULL UP



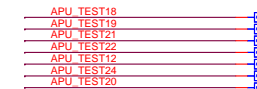
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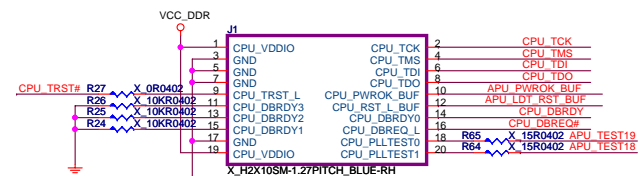
For DVI/HDMI

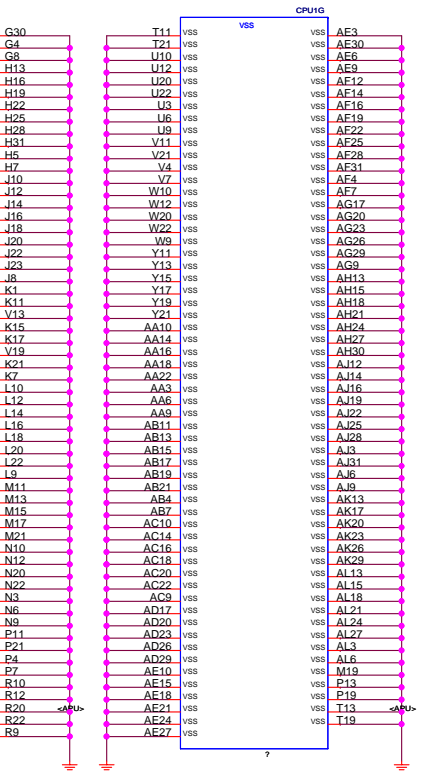
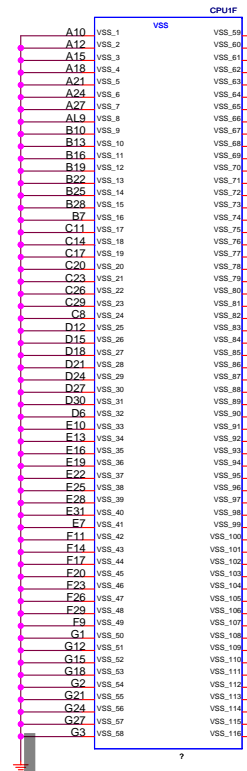
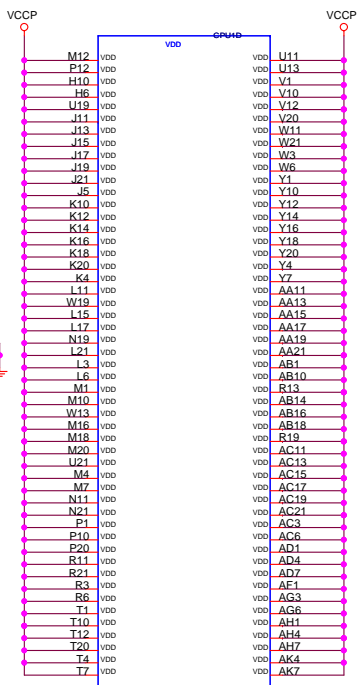
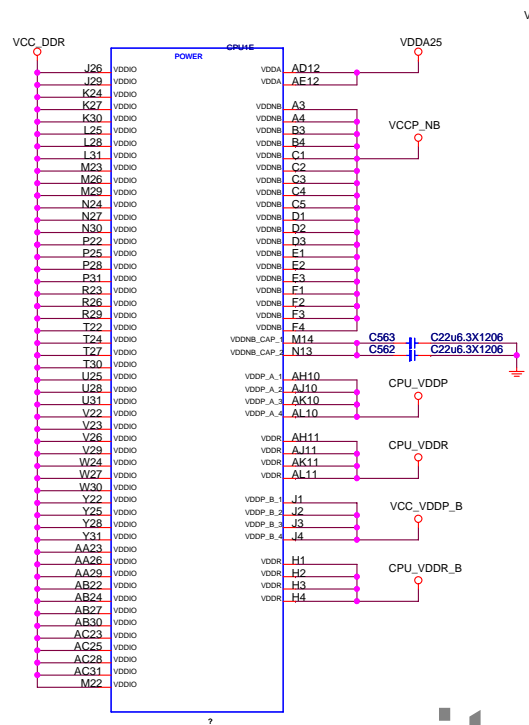
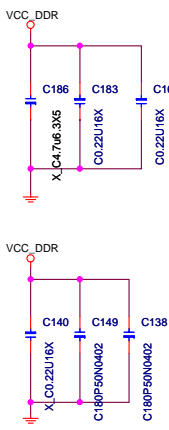
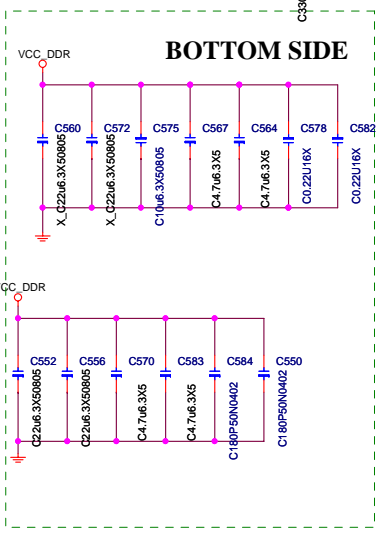
For VGA

SCAN Connector

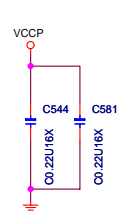
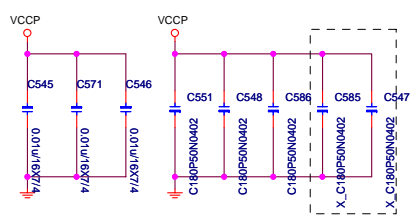
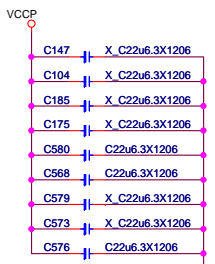
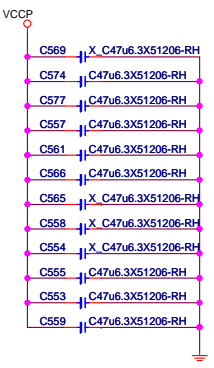


HDT+ Connector



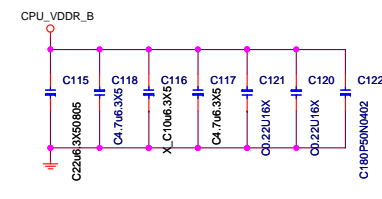
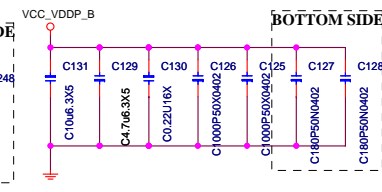
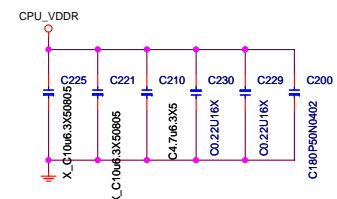
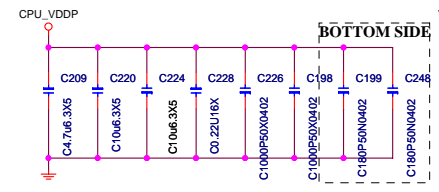


BOTTOM SIDE

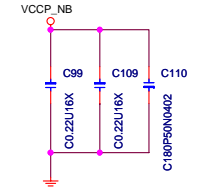
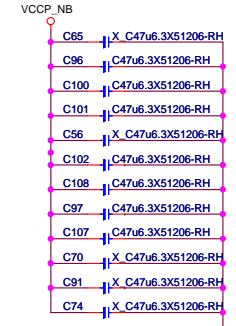


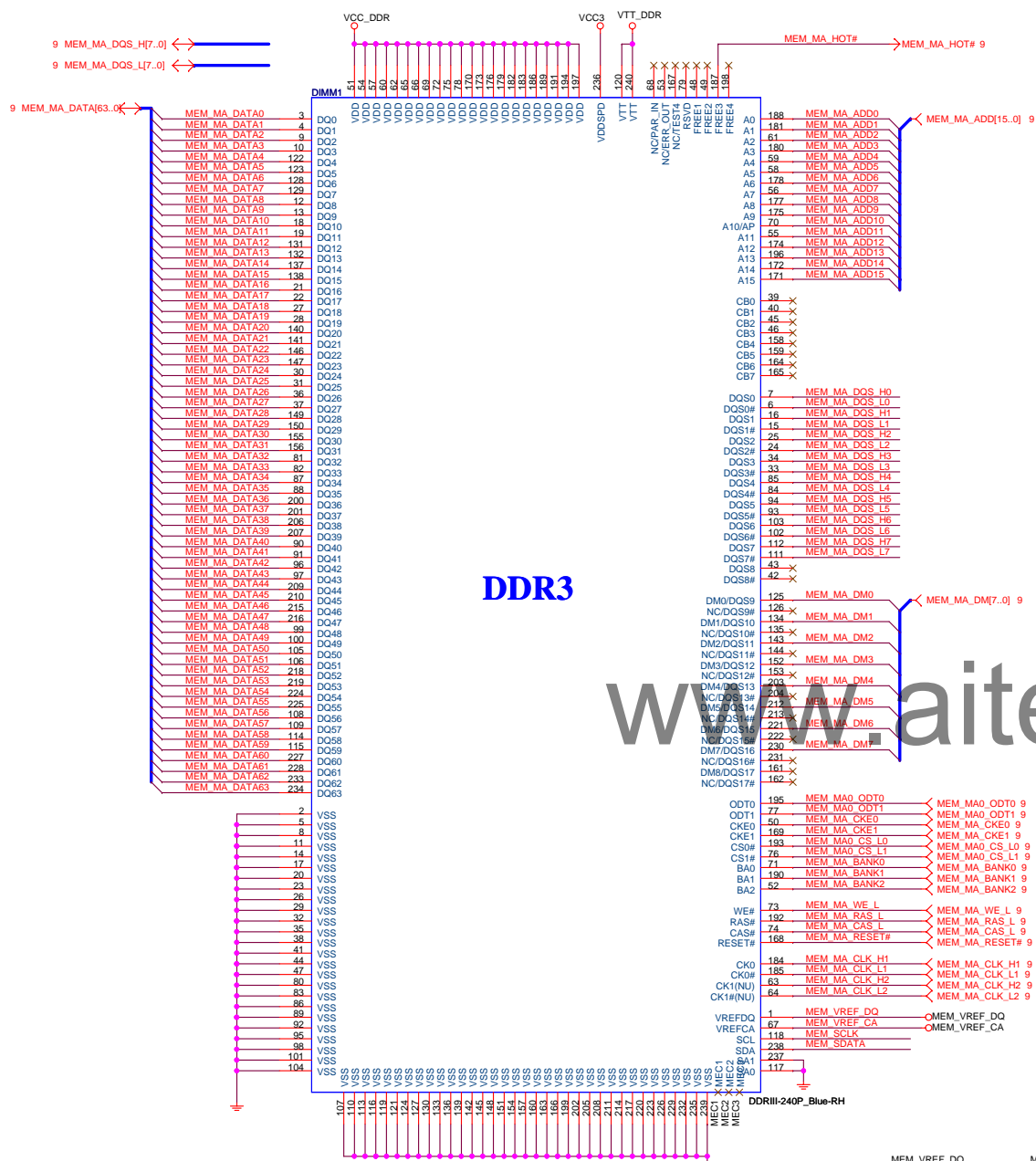
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VDDP and VDDR support two separate power planes with single regulator



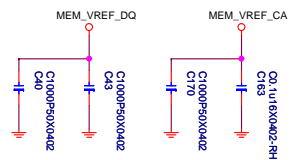
BOTTOM SIDE




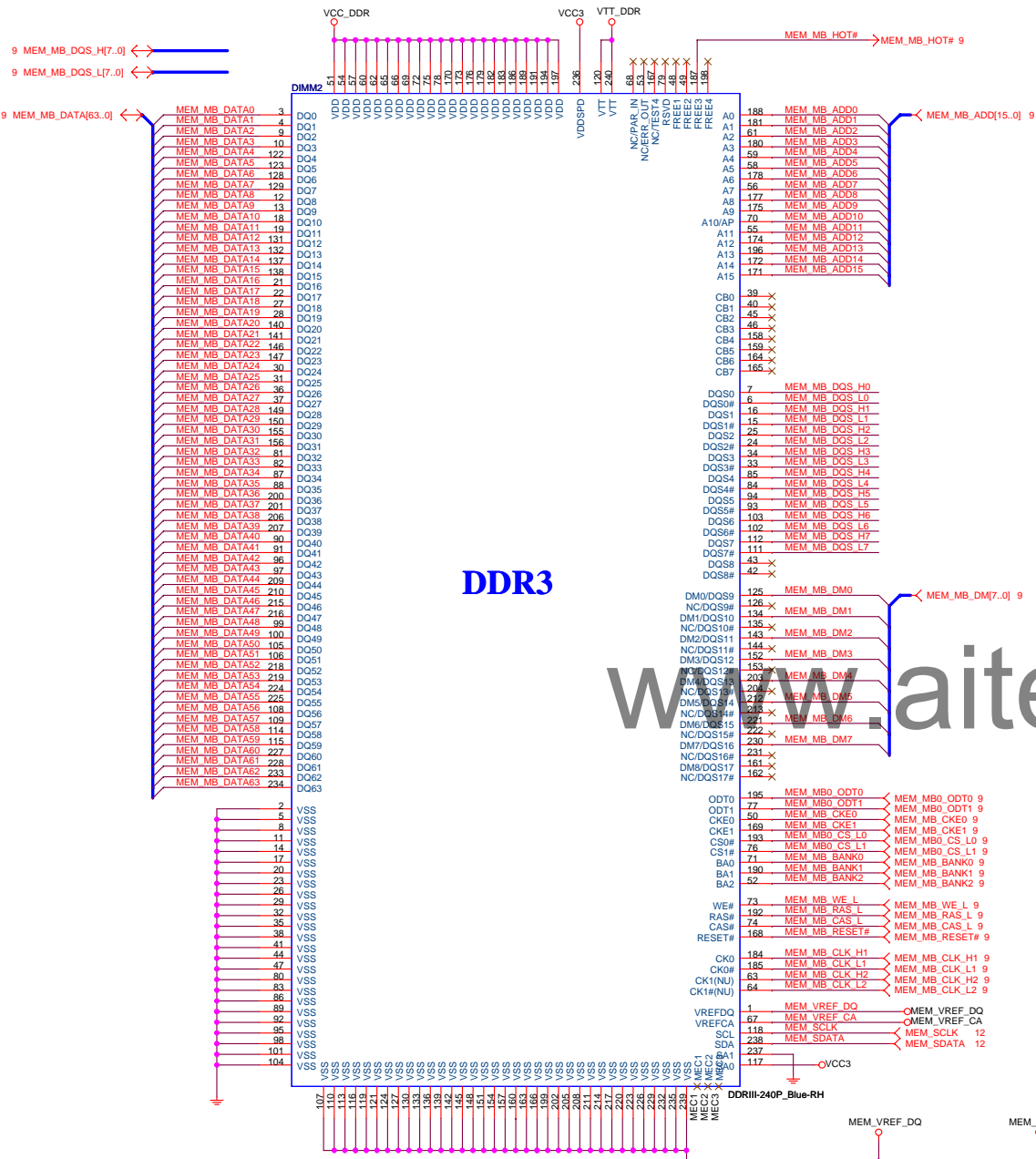


DDR3

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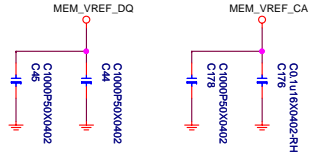
 MICRO-START INT'L CO.,LTD.		
Title: DDR CH-A		
Size: Custom	Document Number: MS-7695	Rev: 1.0
Date: Tuesday, May 31, 2011	Sheet: 12	of: 37



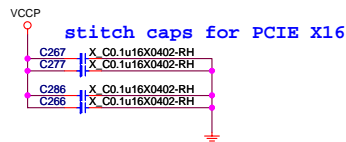
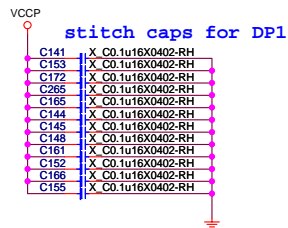
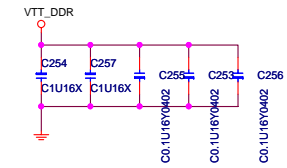
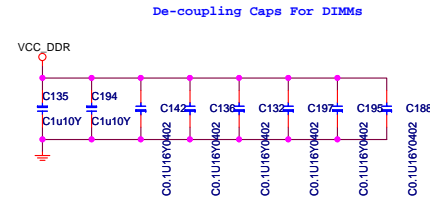
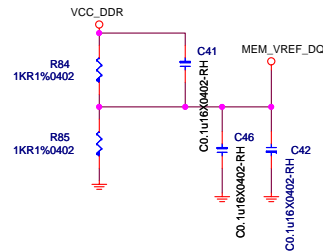
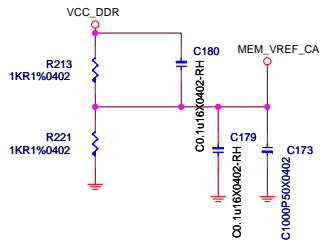
DDR3

DIMM3 (CHANNEL-B B0)
SM ADDRESS=A2

DDRIII-240P_Blue-RH



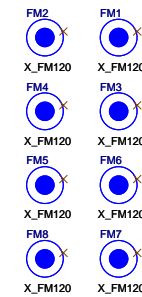
DDR REF POWER & CAPS



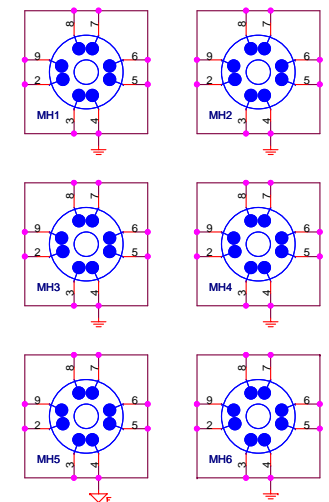
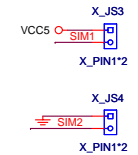
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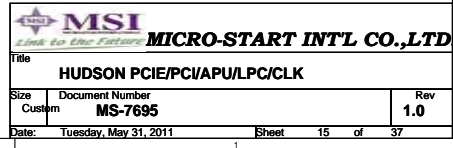
- VCCP
- VCCP_NB
- CPU_VDDR
- CPU_VDDP
- VDDA_25
- VCC_DDR
- VTT_DDR
- VCC1P1
- +1.1VDUAL
- VCC3_SB
- VCC3_WAKE
- VDD10

Optics Orientation Holes

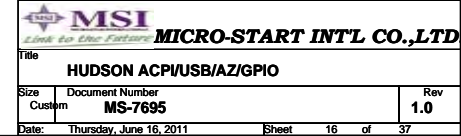


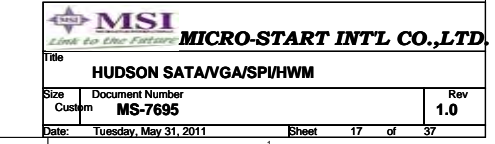
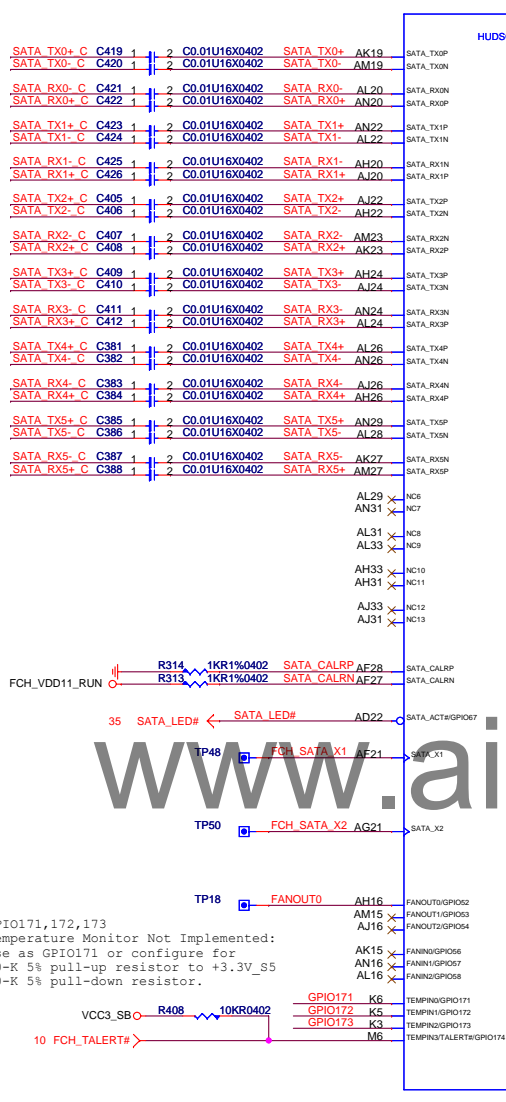
Simulation



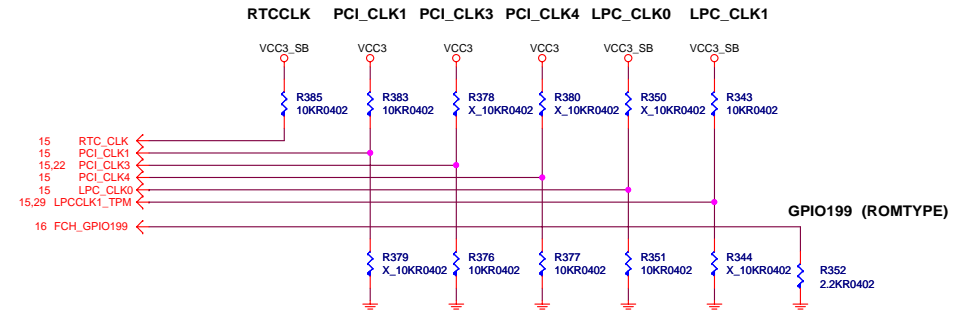
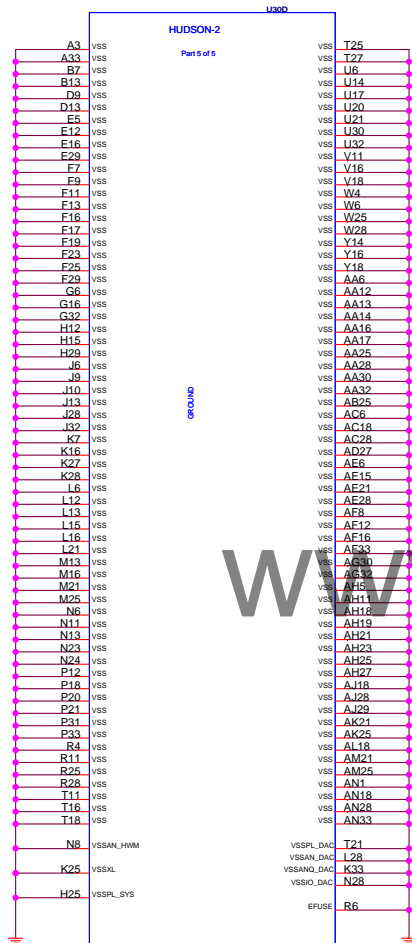


_____ ??????????????????????





FCH REQUIRED STRAPS



	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199 (ROMTYPE)
PULL HIGH	S5 Plus MODE DISABLED DEFAULT	PCIe interface at Gen2 DEFAULT	Enable Debug Straps	Reserved	EC ENABLED	Internal clock mode DEFAULT	LPC ROM
PULL LOW	S5 Plus MODE ENABLED	FORCE PCIe at Gen1	Disable Debug Straps DEFAULT	APU_CLK/DISP_CLK Required setting DEFAULT	EC DISABLED DEFAULT	External clock mode	SPI ROM DEFAULT

*This strap is not used in External clock mode

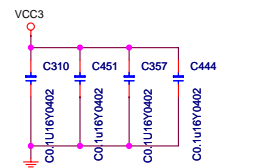
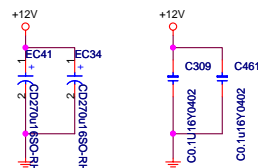
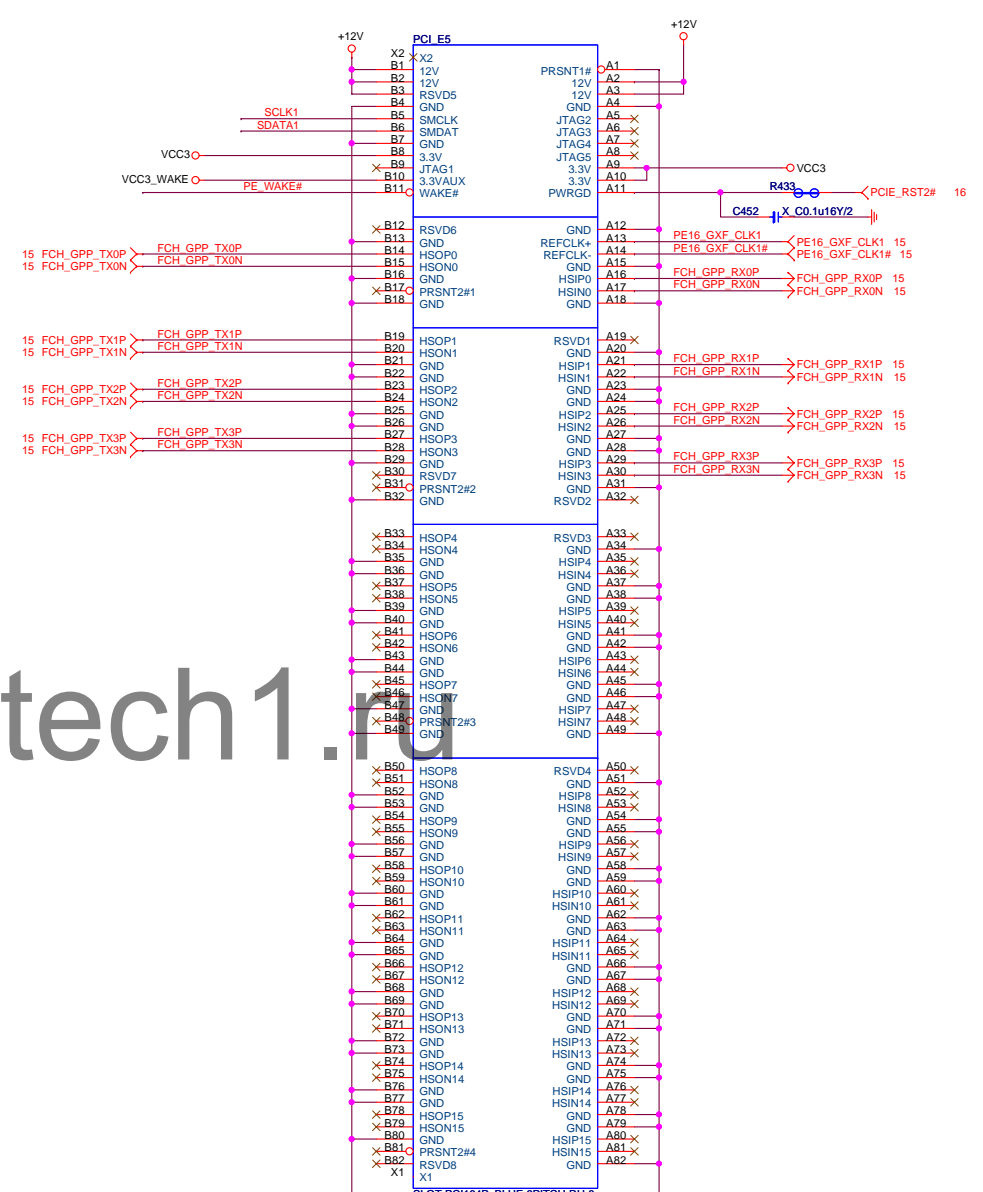
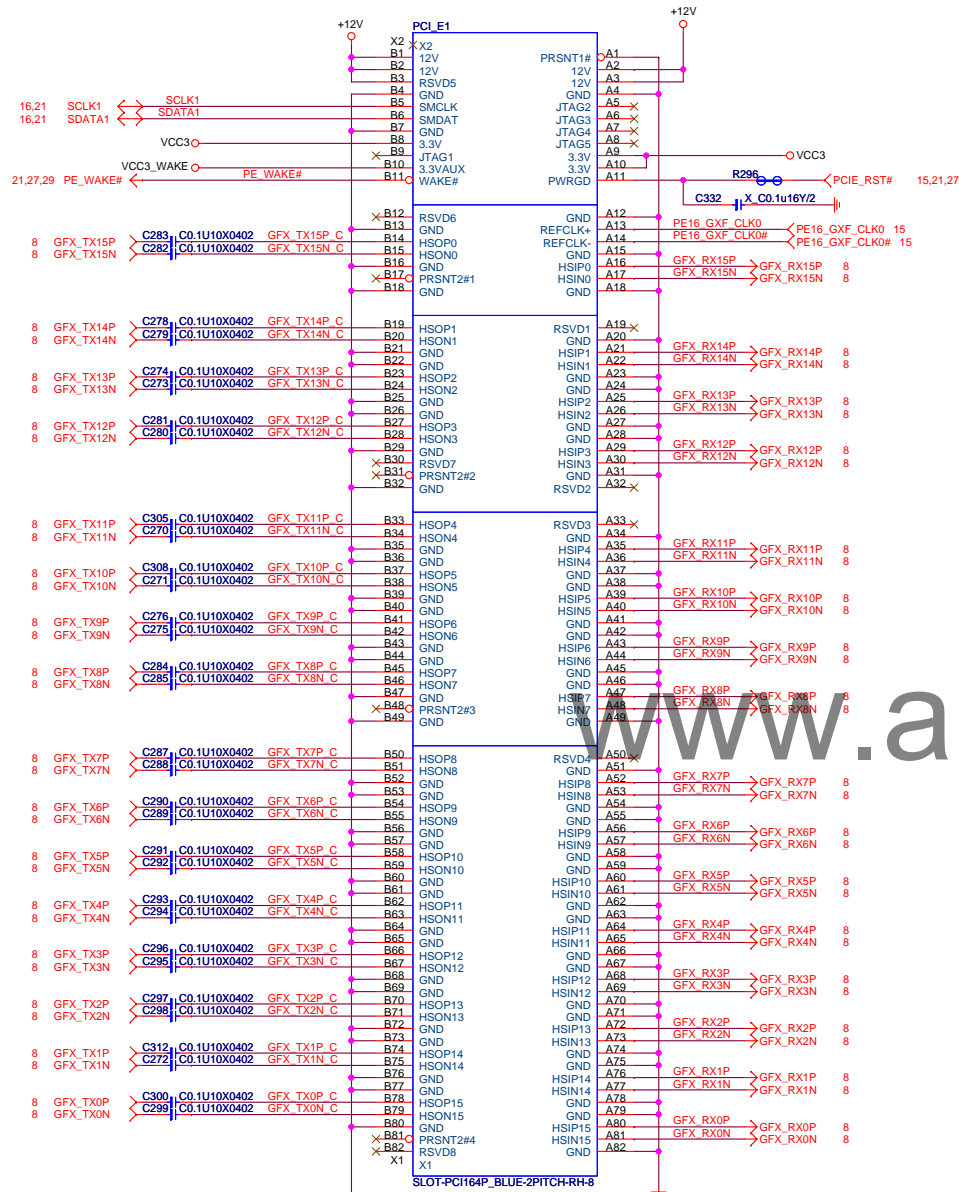
FCH DEBUG STRAPS

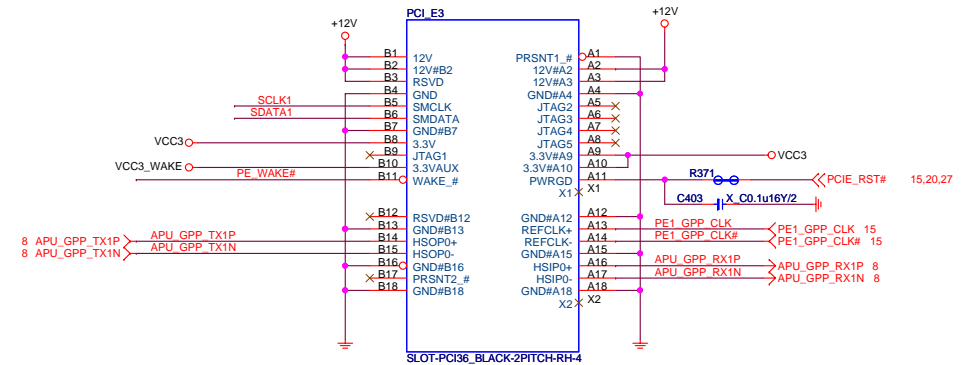
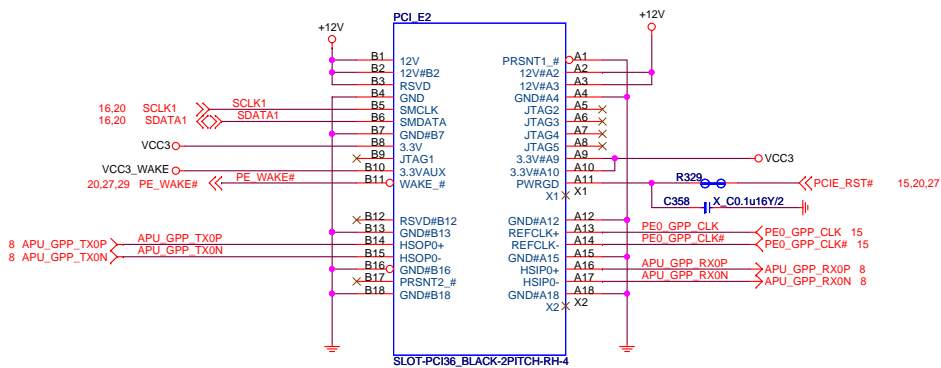


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL clock DEFAULT			Disable I2C ROM DEFAULT	Use ROMTYPE straps DEFAULT
PULL DOWN	Bypass Internal PLL clock			Enable loading settings for UMI/PLL/misc from I2C ROM	Boot from PCI bus

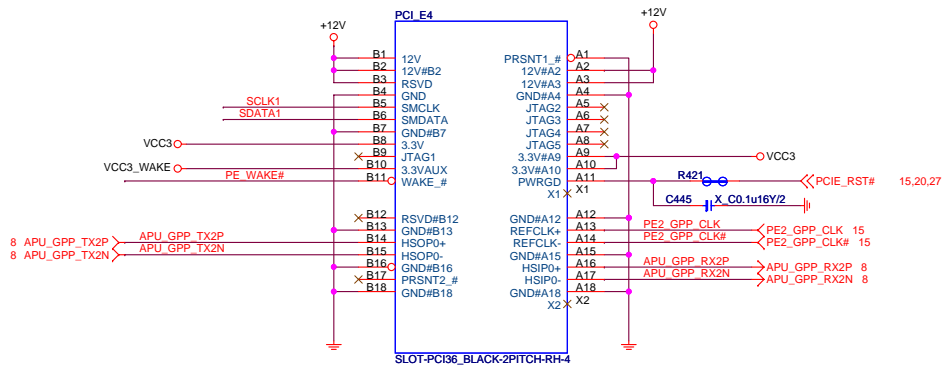
Layout:
VSSPL_SYS/VSSAN_HMM CONNECT TO GND
WITH A SEPERATED VIA

PCI EXPRESS x16 Slot

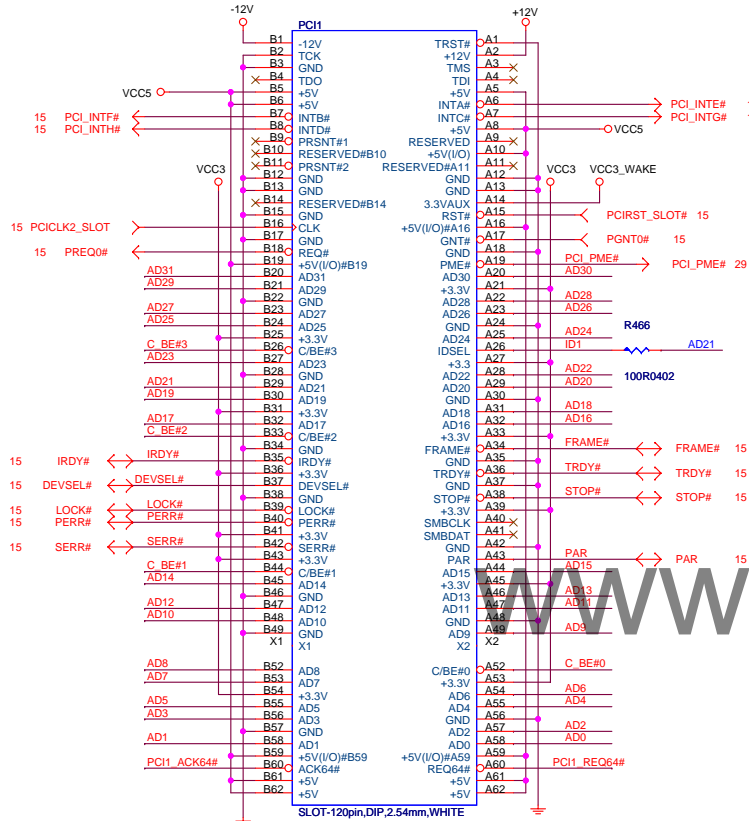




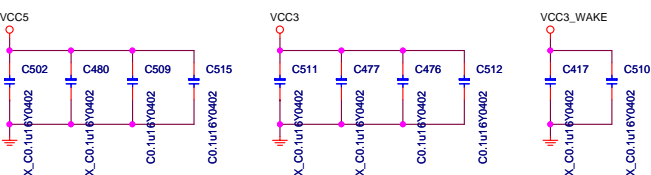
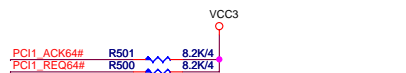
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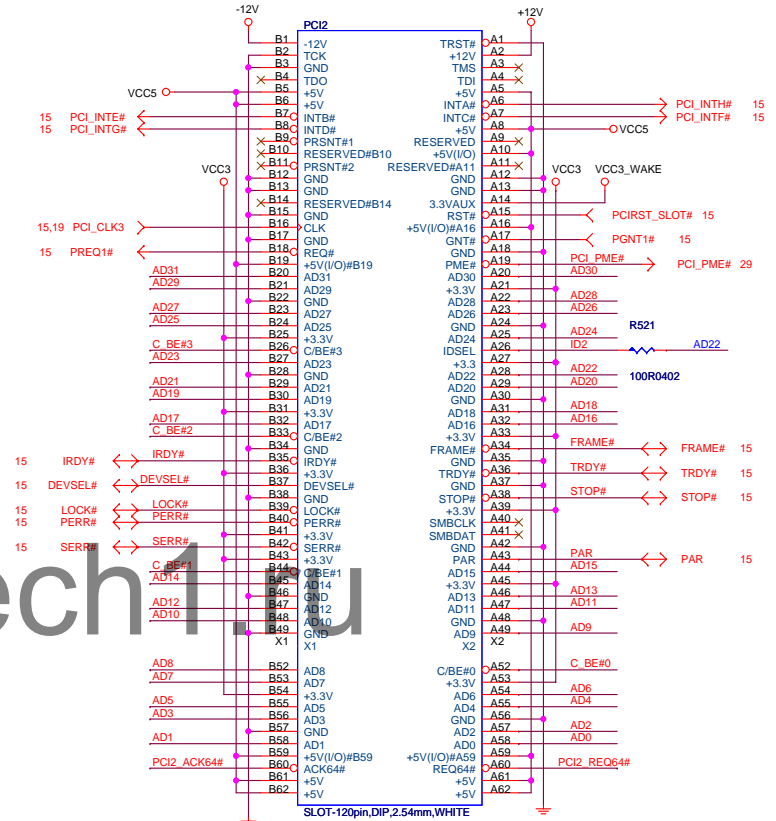
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



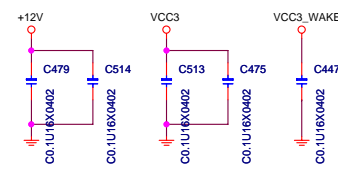
ISSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0



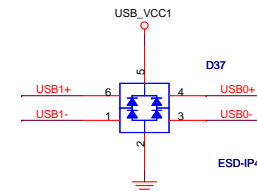
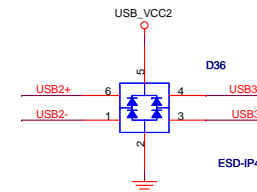
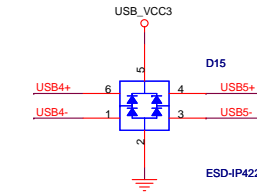
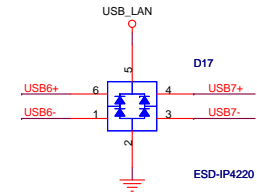
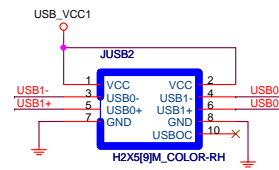
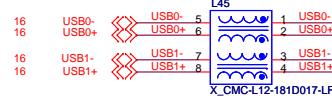
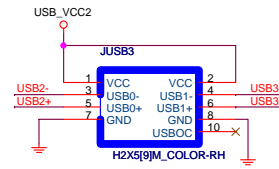
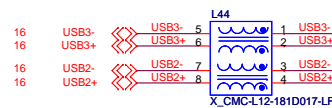
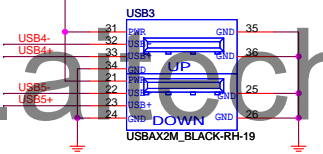
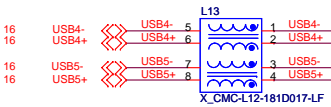
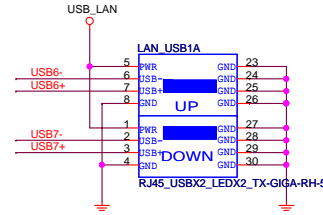
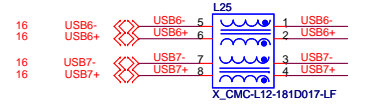
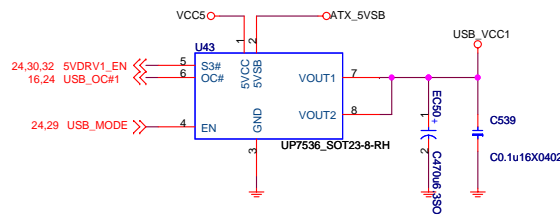
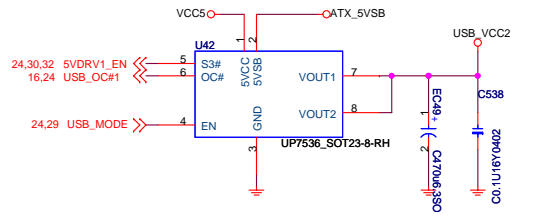
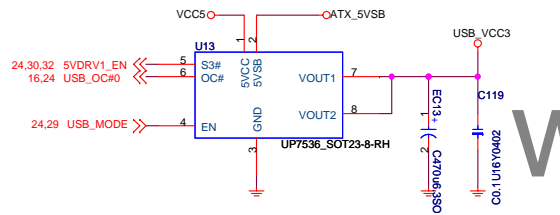
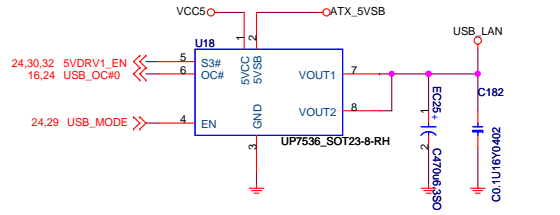
PCI SLOT 2 (PCI VER: 2.2 COMPLY)

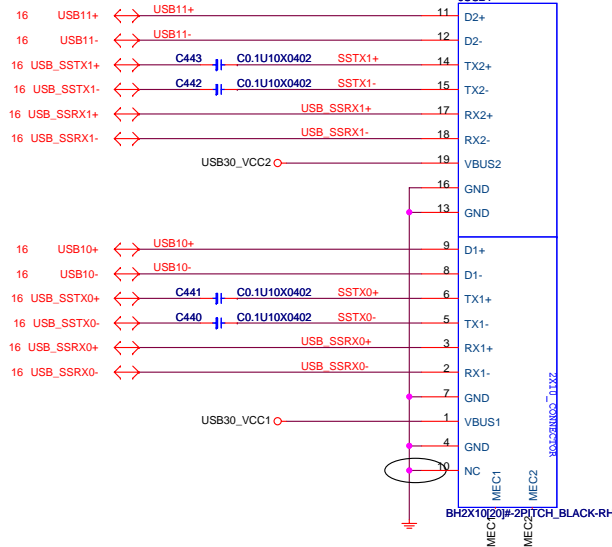
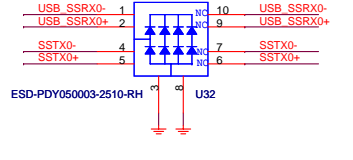
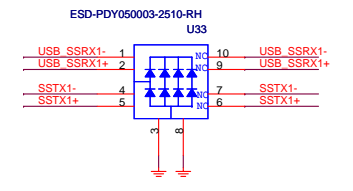
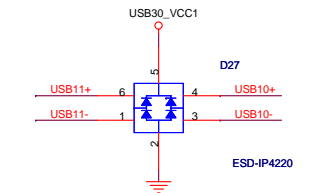
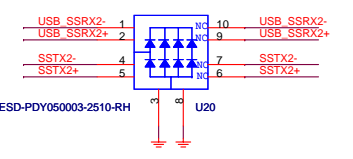
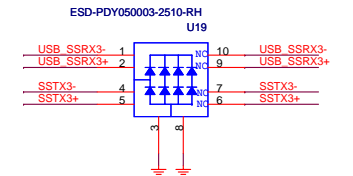
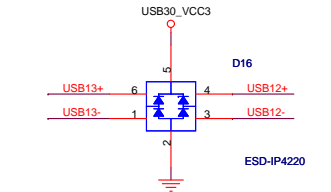
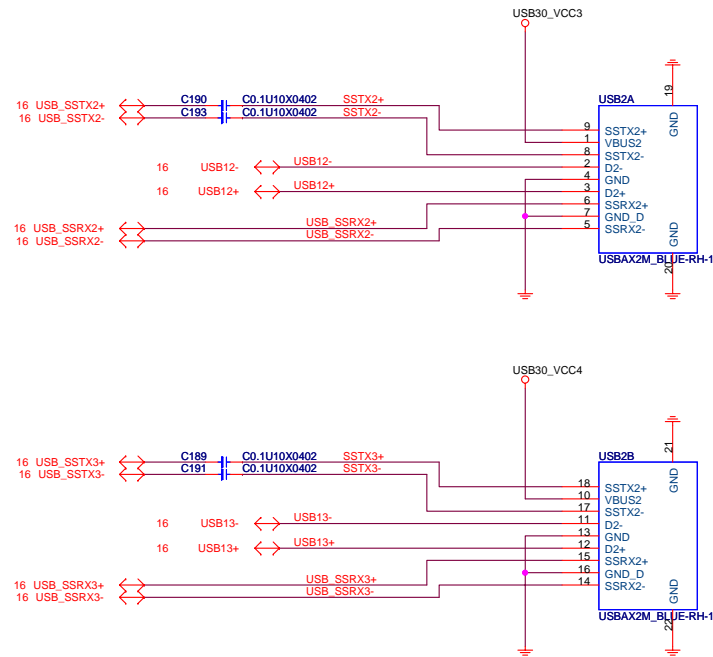
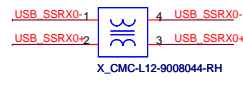
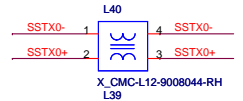
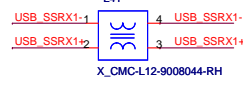
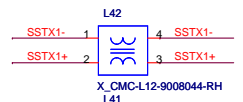
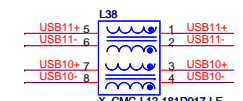
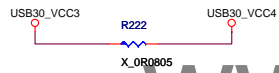
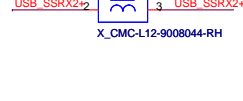
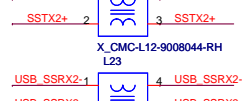
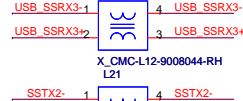
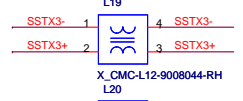
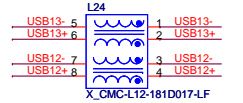
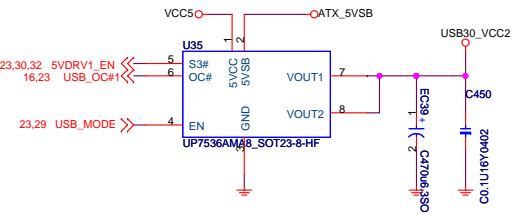
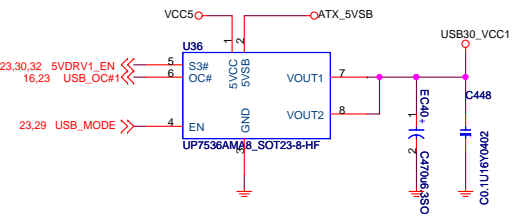
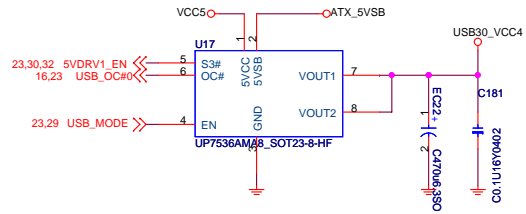
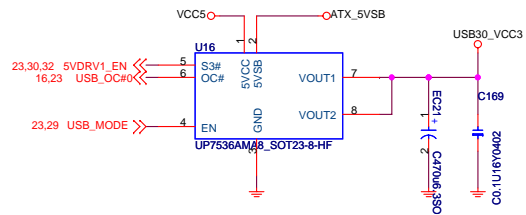


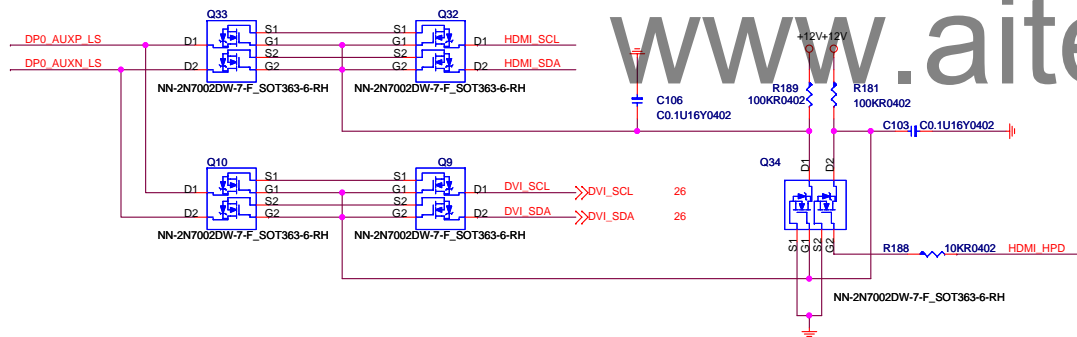
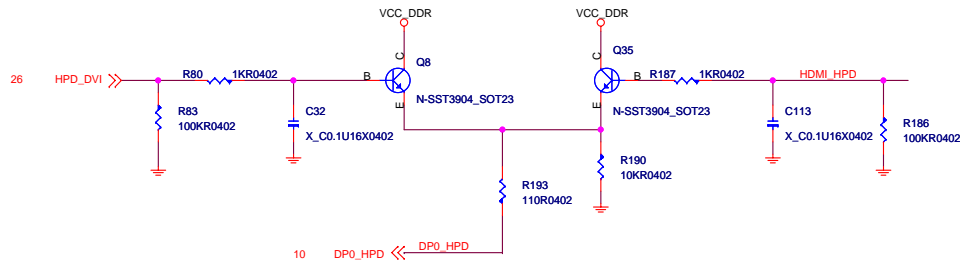
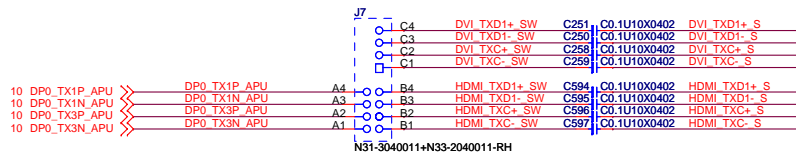
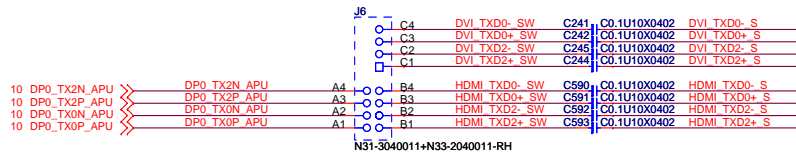
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MASTER = PCI_REQ#1
PCI_GNT#1



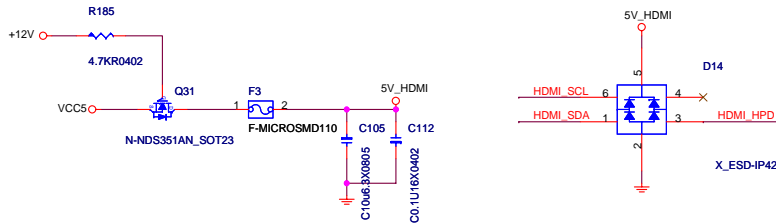
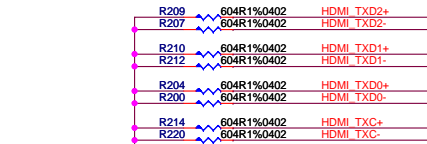
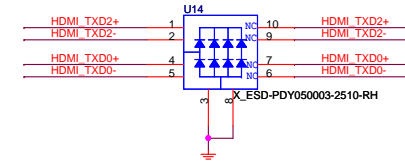
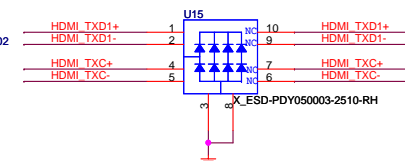
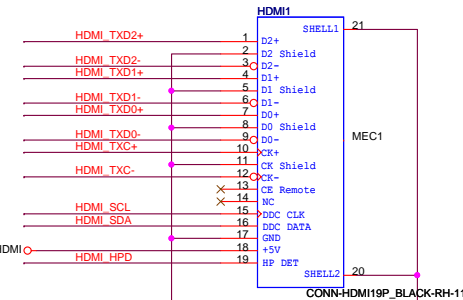
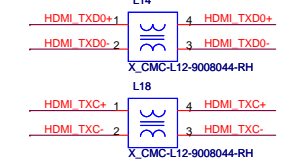
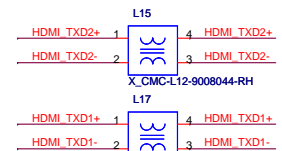
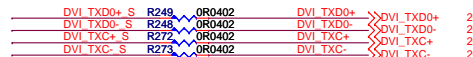
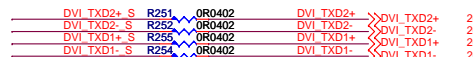
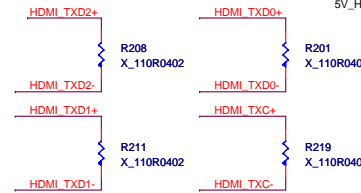
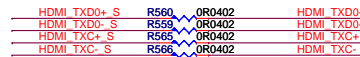
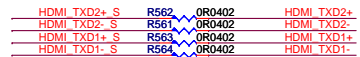
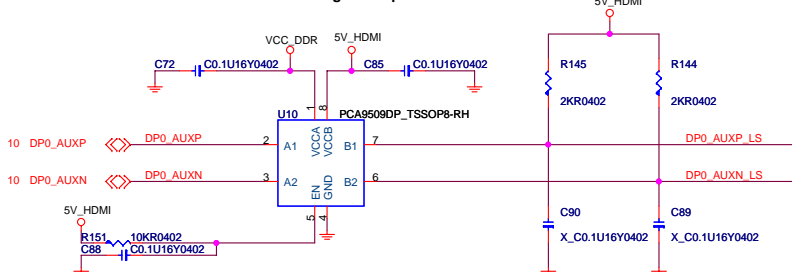
POWER CIRCUIT FOR USB PORT 0,1



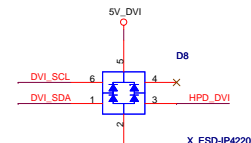
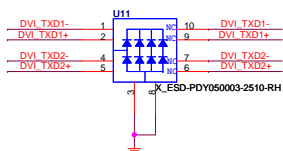
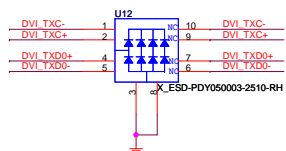
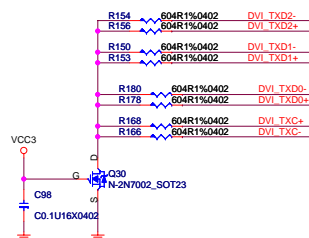
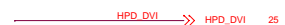
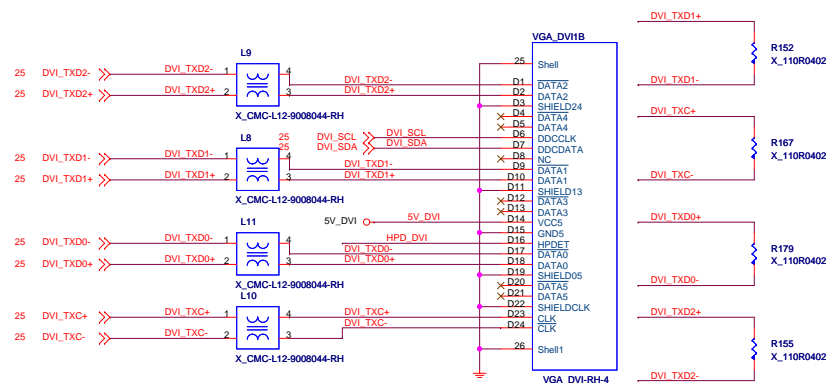




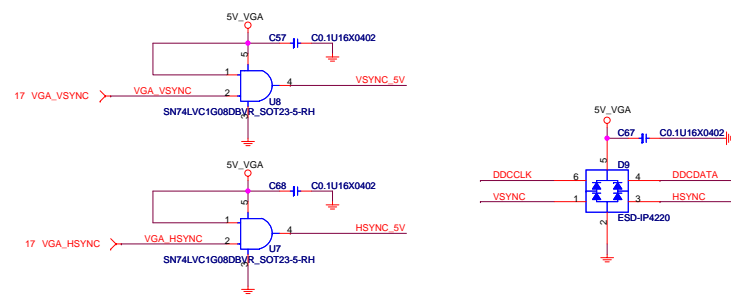
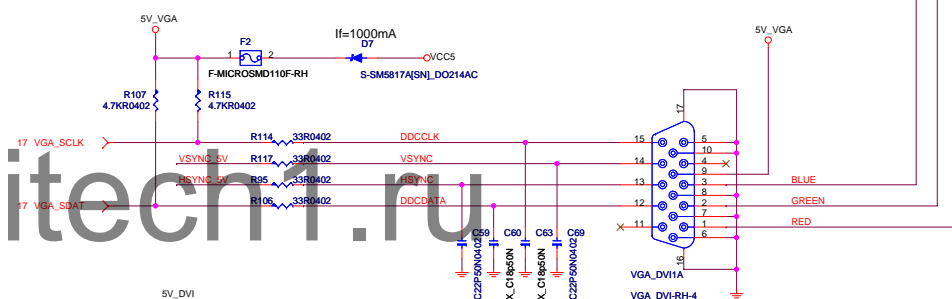
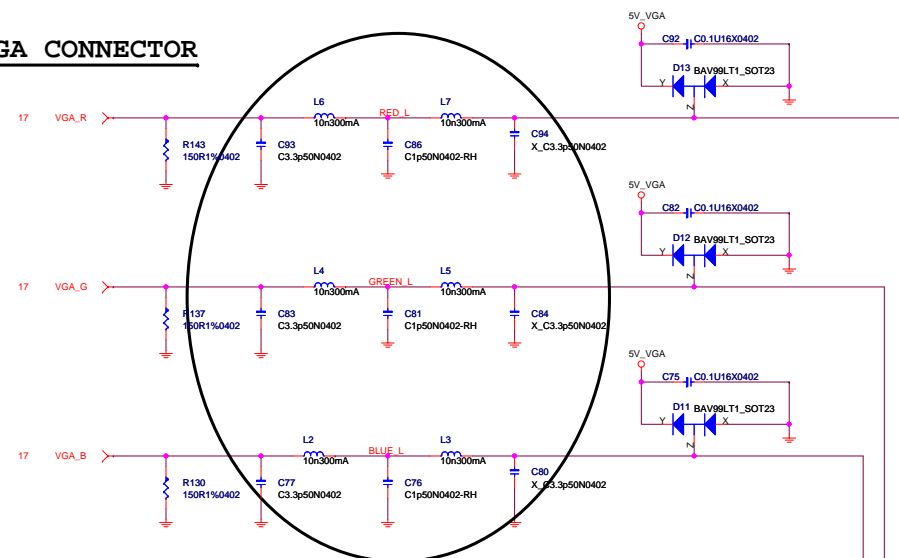
LEVEL SHIFT using I2C Repeater

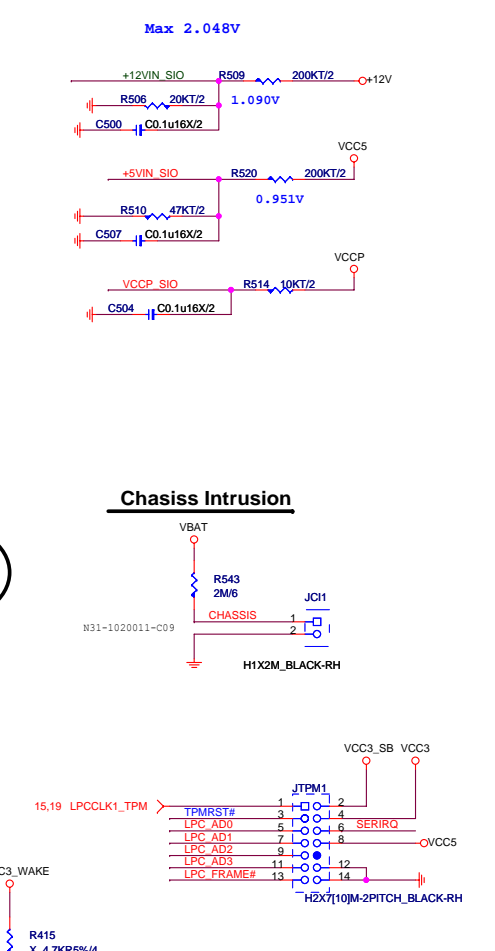
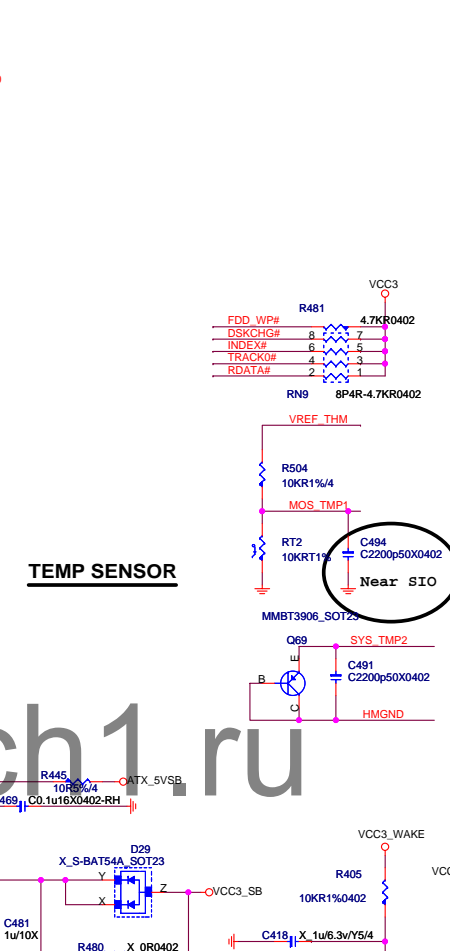
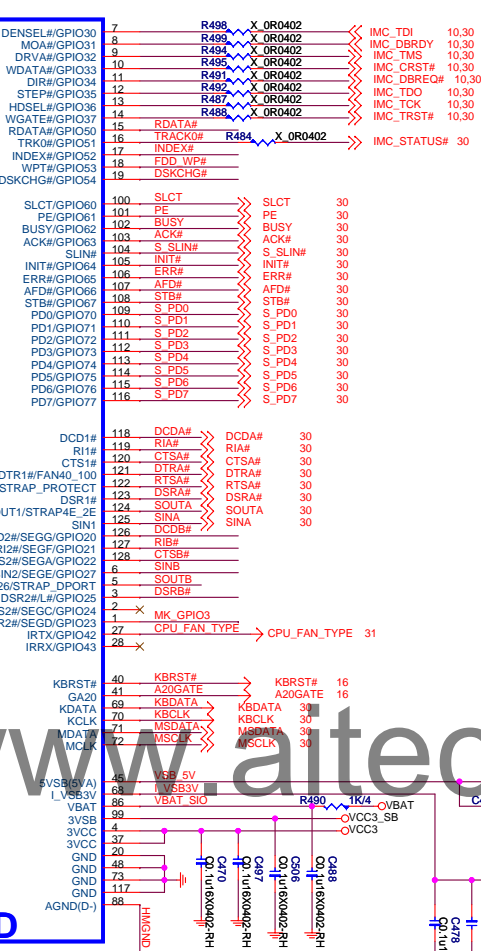
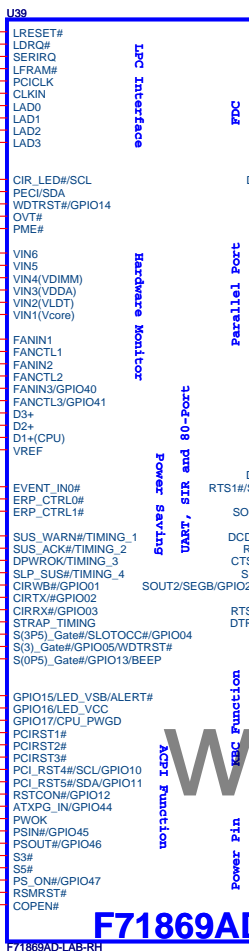
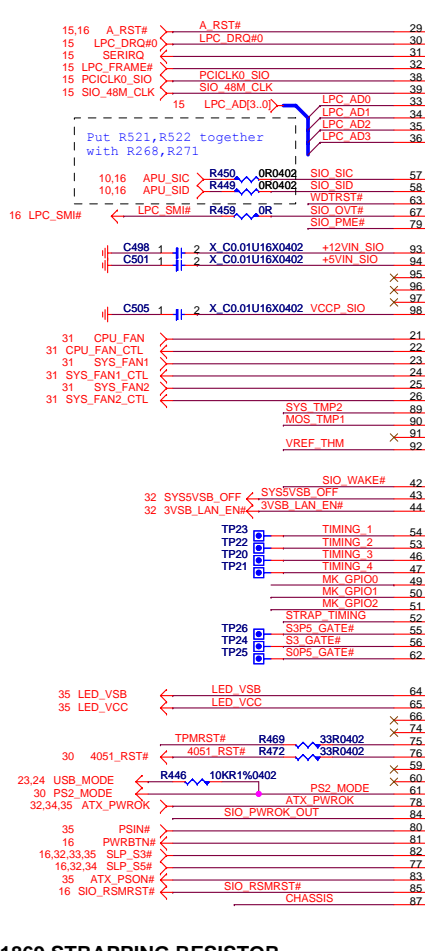


DVI CONNECTOR

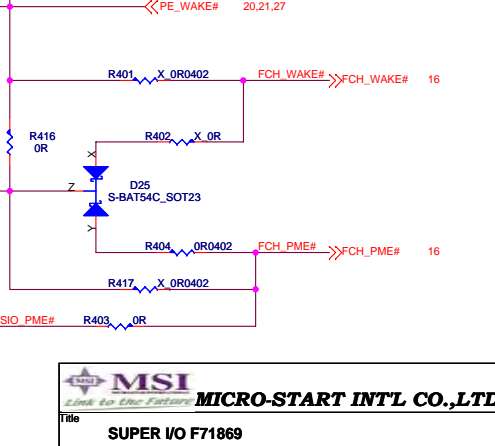
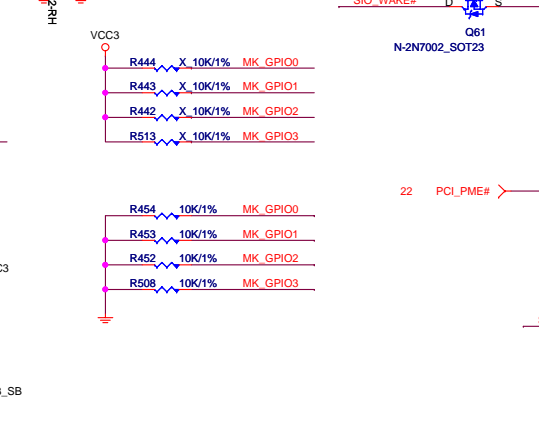
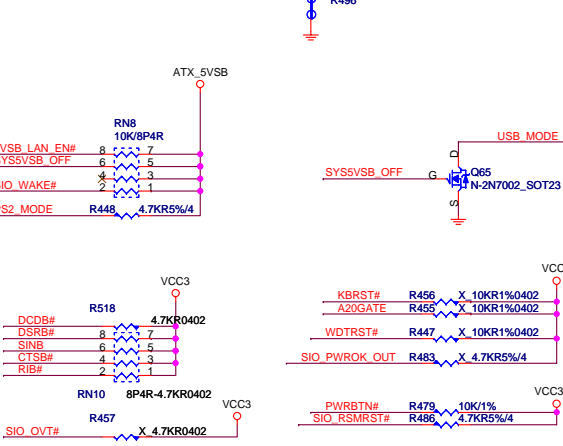
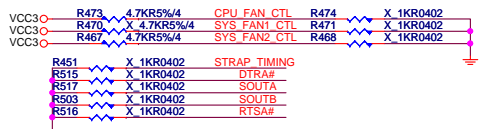


VGA CONNECTOR



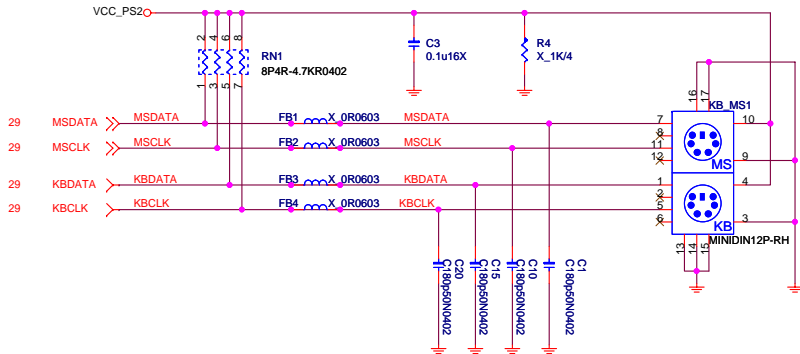
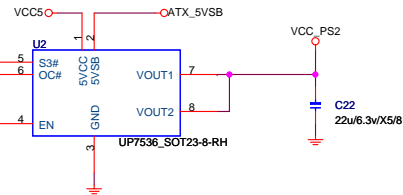
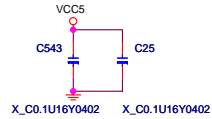
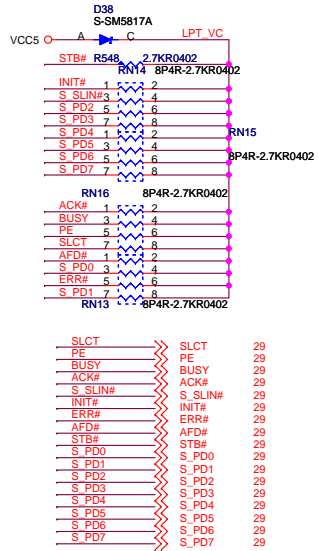


F71869 STRAPPING RESISTOR

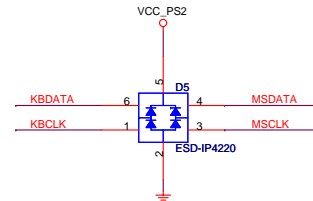
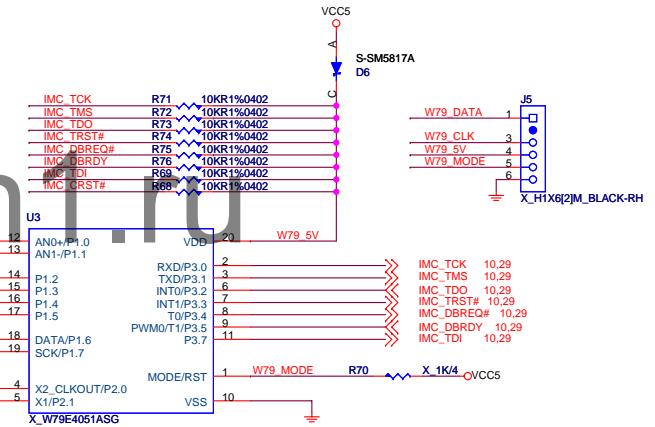
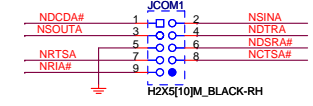
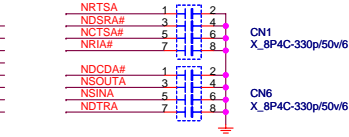
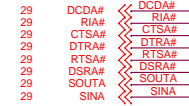
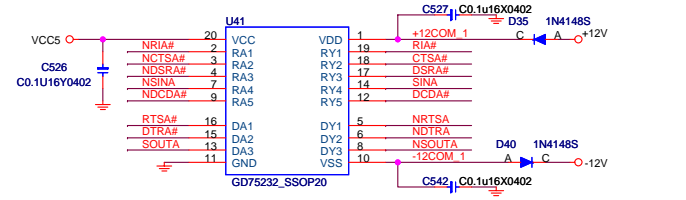


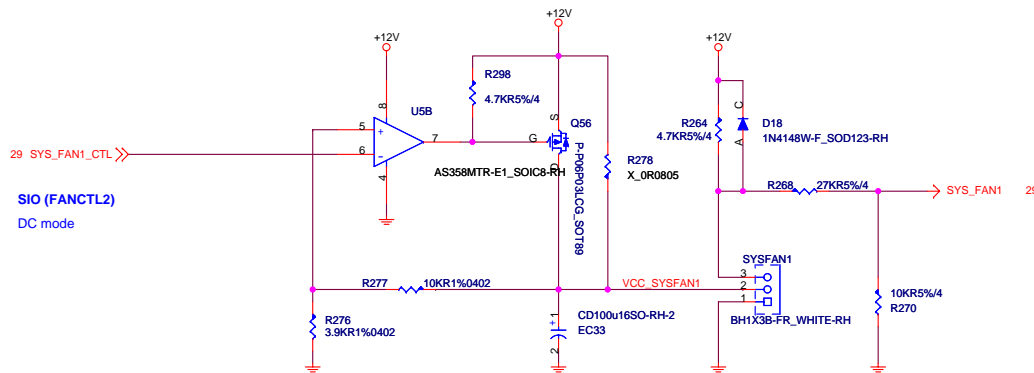
	1	0
STRAP_TIMING	AMD	Intel
DTRA#	FAN start duty is 40%	FAN start duty is 100%
SOUTA	4E	2E
FANCTL1	PWM mode	DAC mode(default)
FANCTL2	PWM mode	DAC mode(default)
FANCTL3	PWM mode	DAC mode(default)
SOUTB	80Port decode output from COM2	COM2
RTSA#	Disable UVP protection	Enable UVP protection

PARALLEL PORT

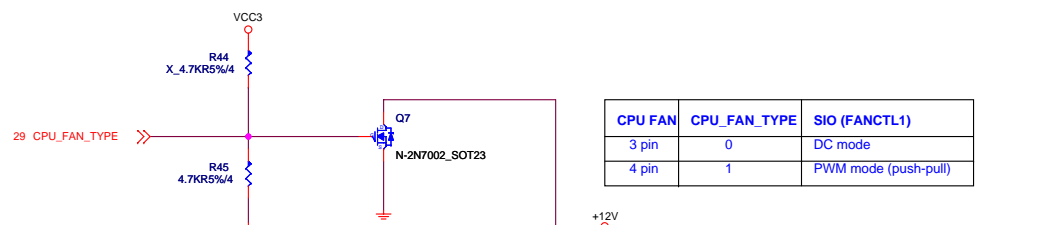


SERIAL PORT 1

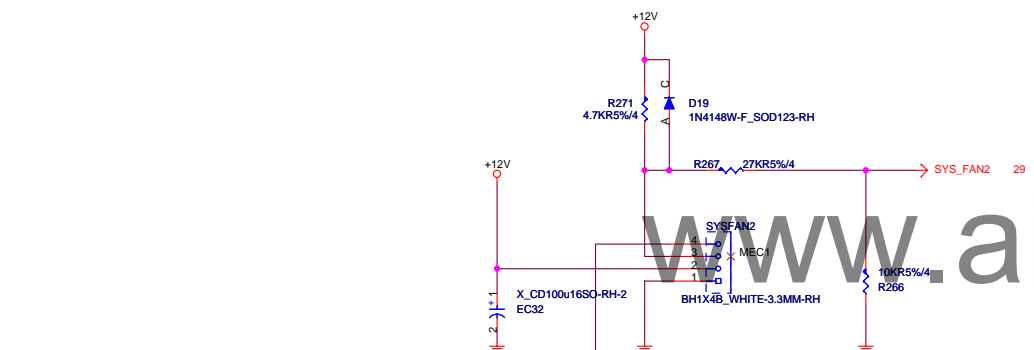




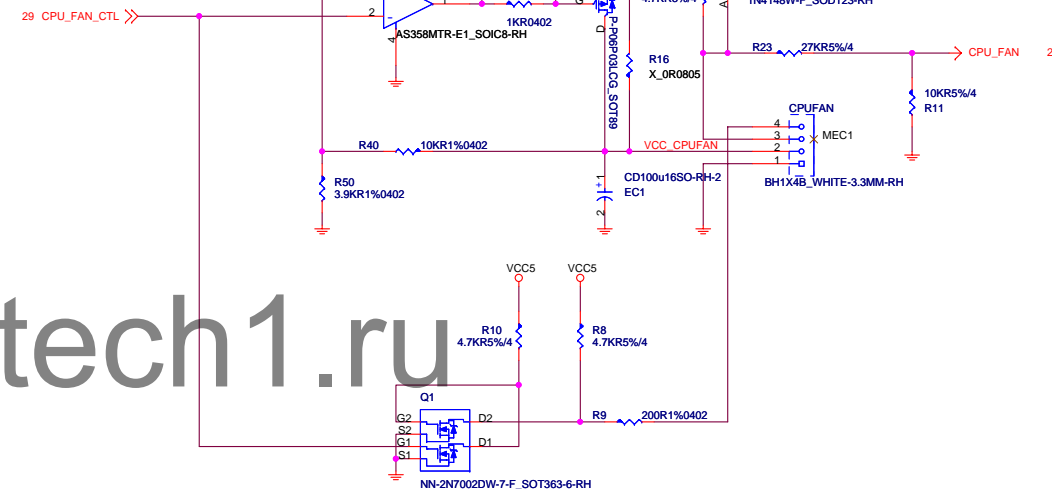
SIO (FANCTL2)
DC mode



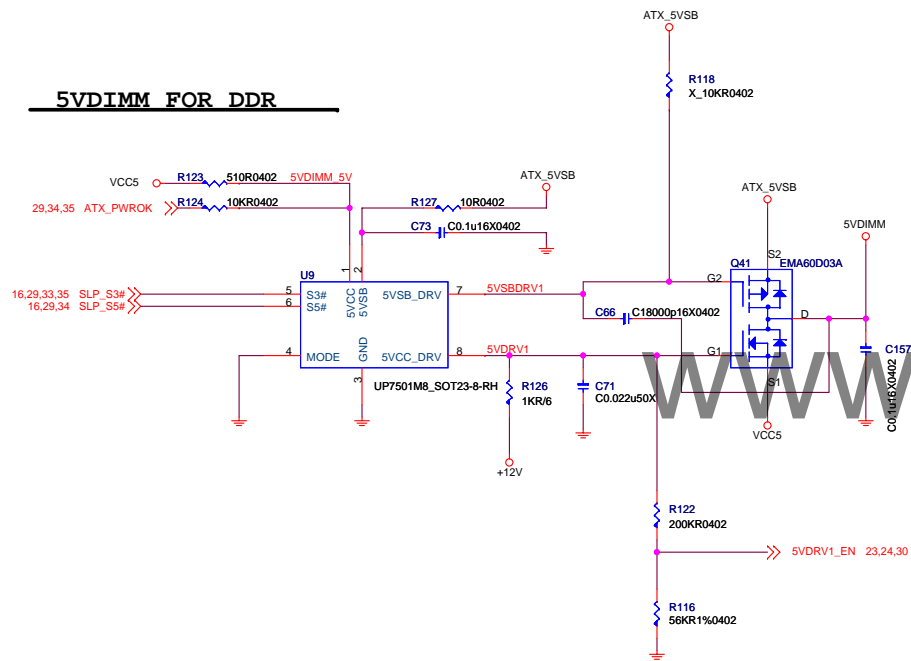
CPU FAN	CPU_FAN_TYPE	SIO (FANCTL1)
3 pin	0	DC mode
4 pin	1	PWM mode (push-pull)



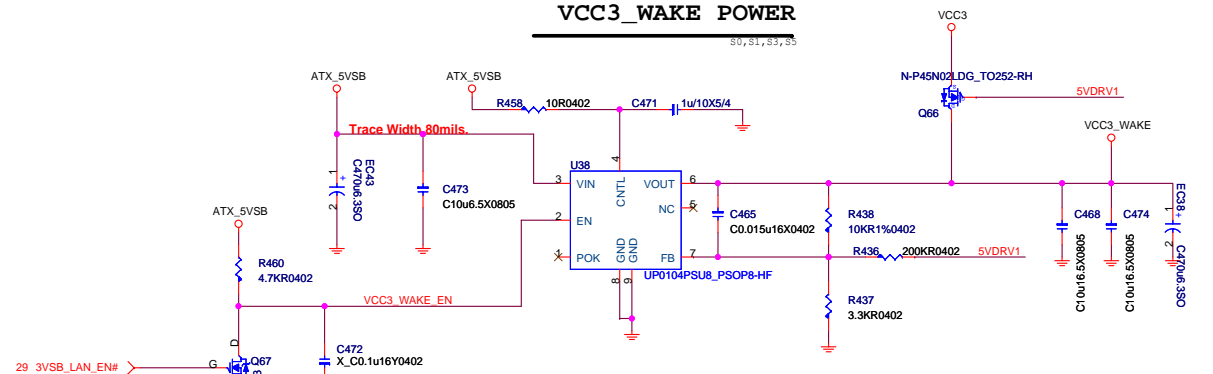
SIO (FANCTL3)
PWM mode



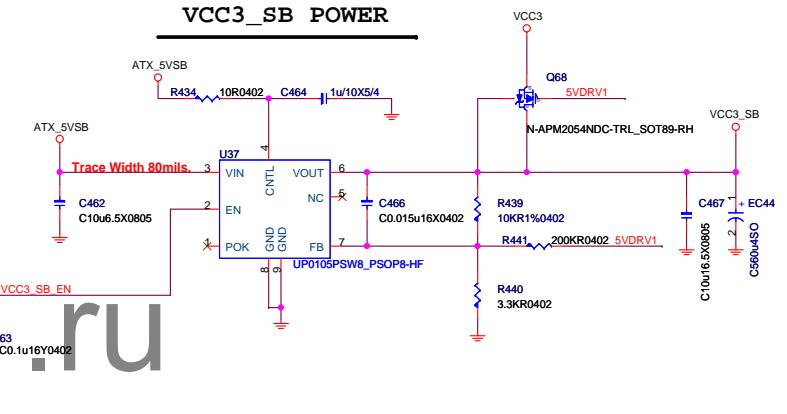
5VDIMM FOR DDR



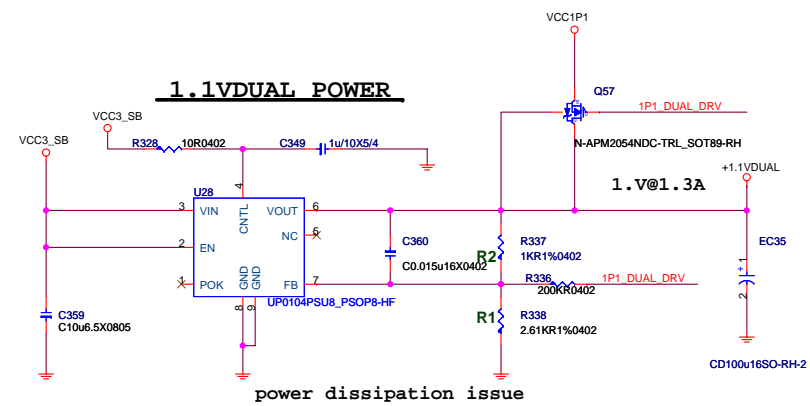
VCC3_WAKE POWER



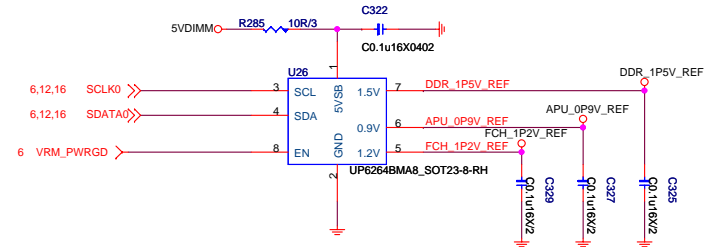
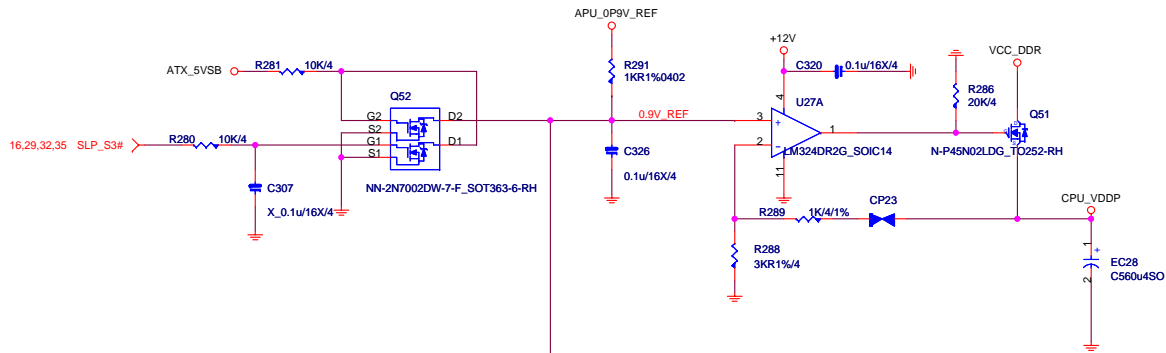
VCC3_SB POWER



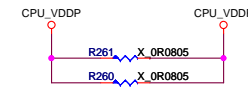
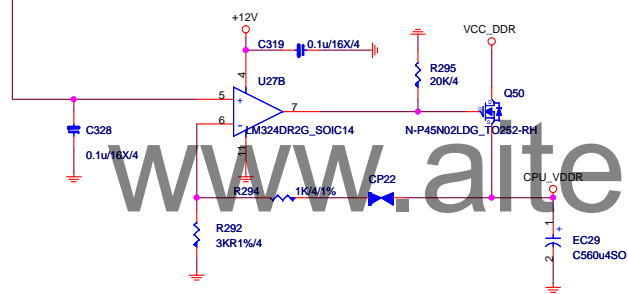
1.1VDUAL POWER



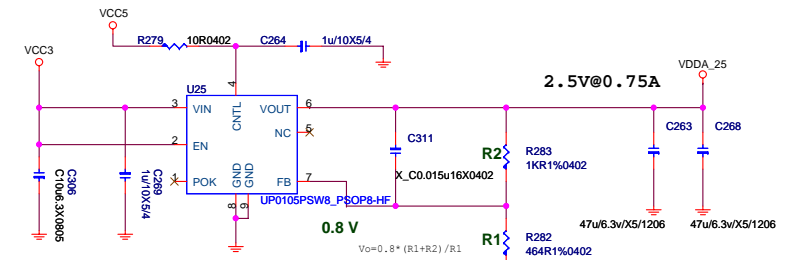
CPU VDDP POWER 1.2 V@3.5A



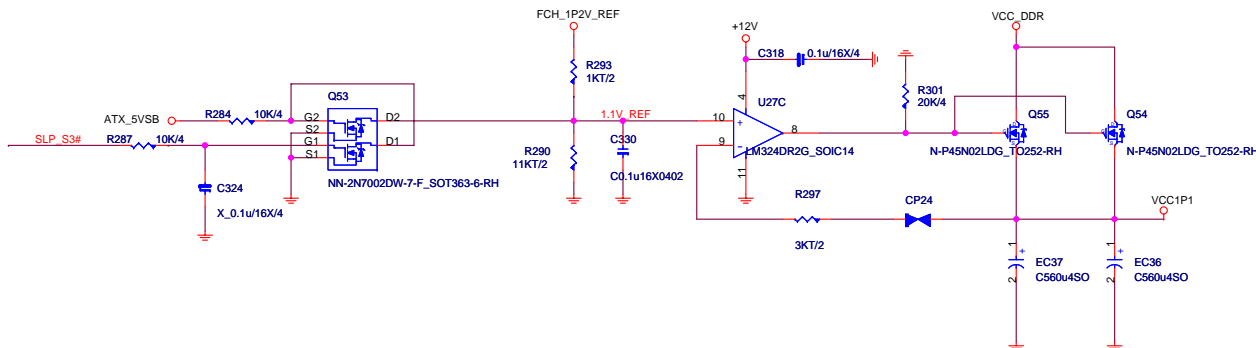
CPU VDDR POWER 1.2 V@4A



CPU VDDA_25 POWER

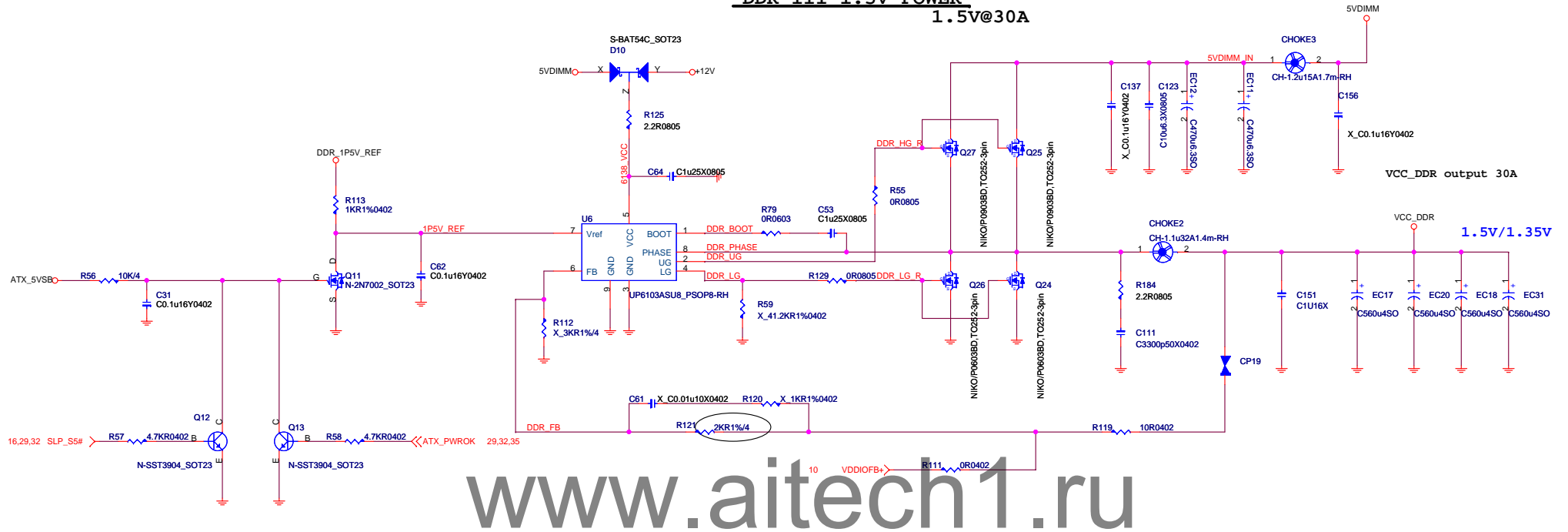


VCC1P1 POWER 1.1V@4.5A+1.3A

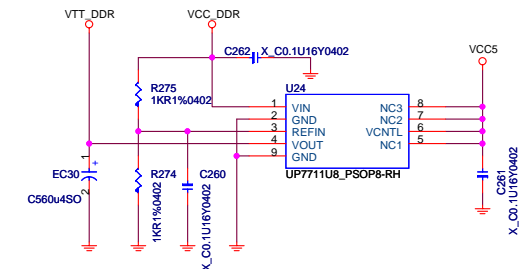


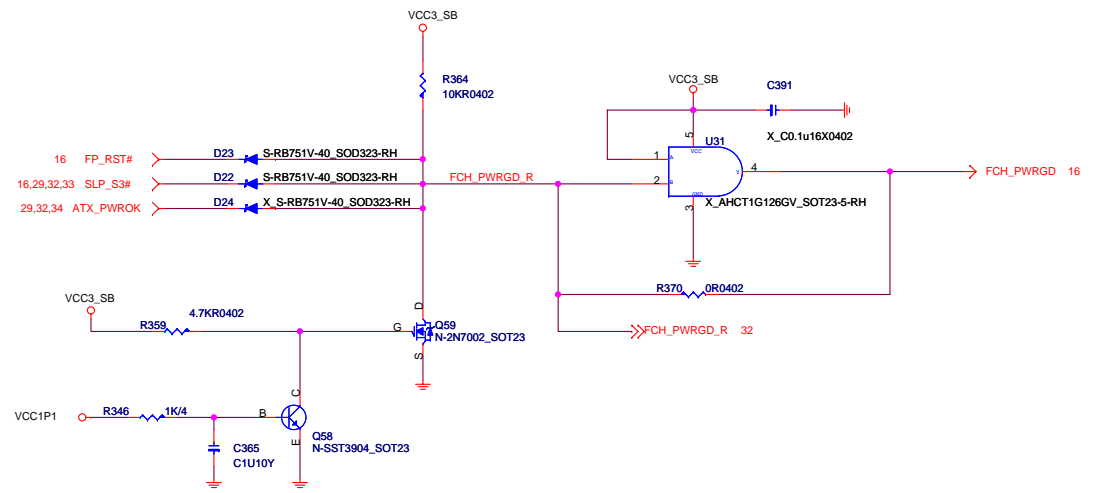
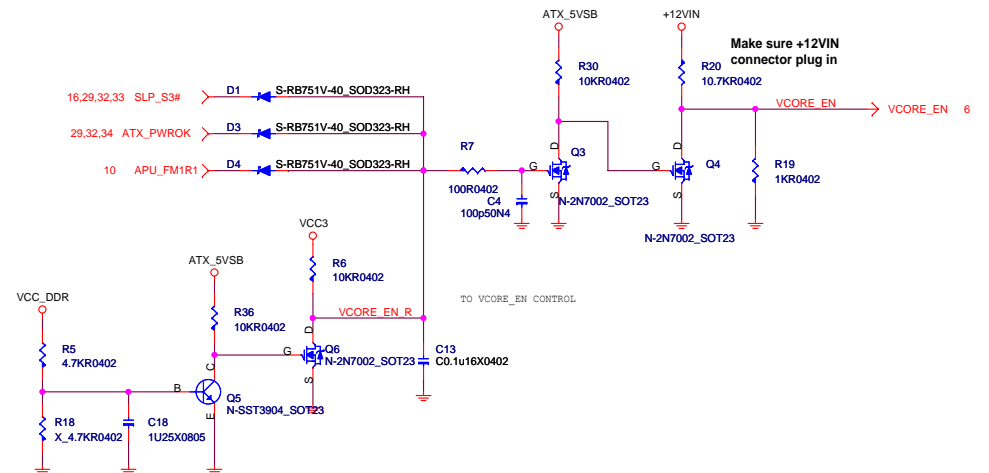
DDR III 1.5V POWER

1.5V@30A

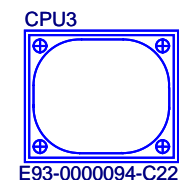
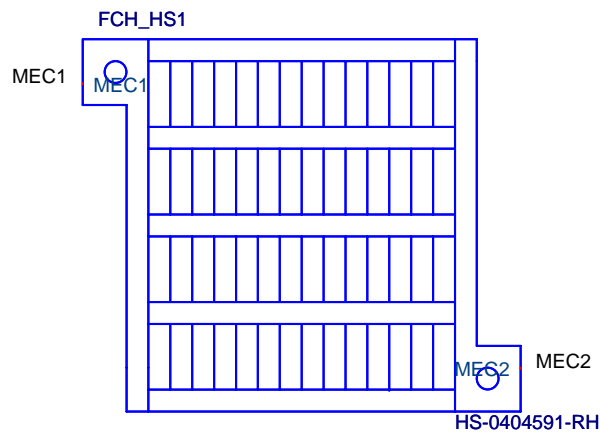


0.75V@2A VTT_DDR POWER

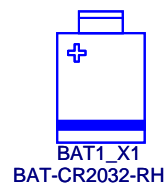


[illegible]

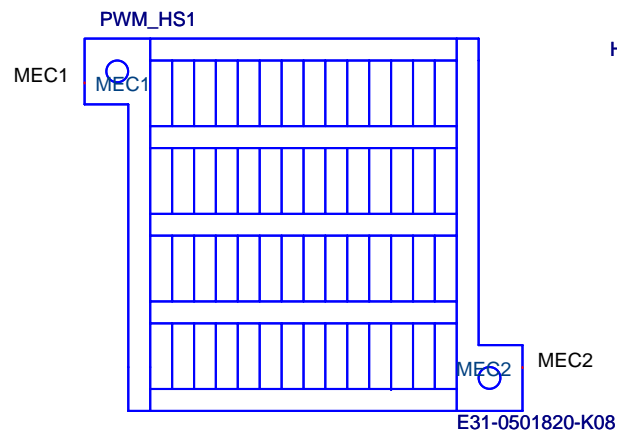
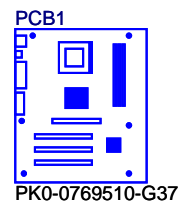
HEAT SINK



MANUAL PART



AVL:
D06-0100161-F52
D06-0100101-K26




Rubber1

OPT

Rubber2


OPT

MK1
G51-M1SPA35-Q13

 MSI Link to the Future MICRO-START INT'L CO.,LTD.		
Title BOM OPTION		
Size A	Document Number MS-7695	Rev 1.0
Date:	Thursday, June 23, 2011	Sheet 36 of 37

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- 1.update VRM chip footprint
- 2.Delete DVI caps
- 3.Updata JTPM1 footprint
- 4.Add R795,R796

 MICRO-START INT'L CO.,LTD.		
Title Auto BOM Mnaual/History		
Size Custom	Document Number MS-7695	Rev 1.0
Date: Tuesday, May 31, 2011	Sheet 37 of 37	